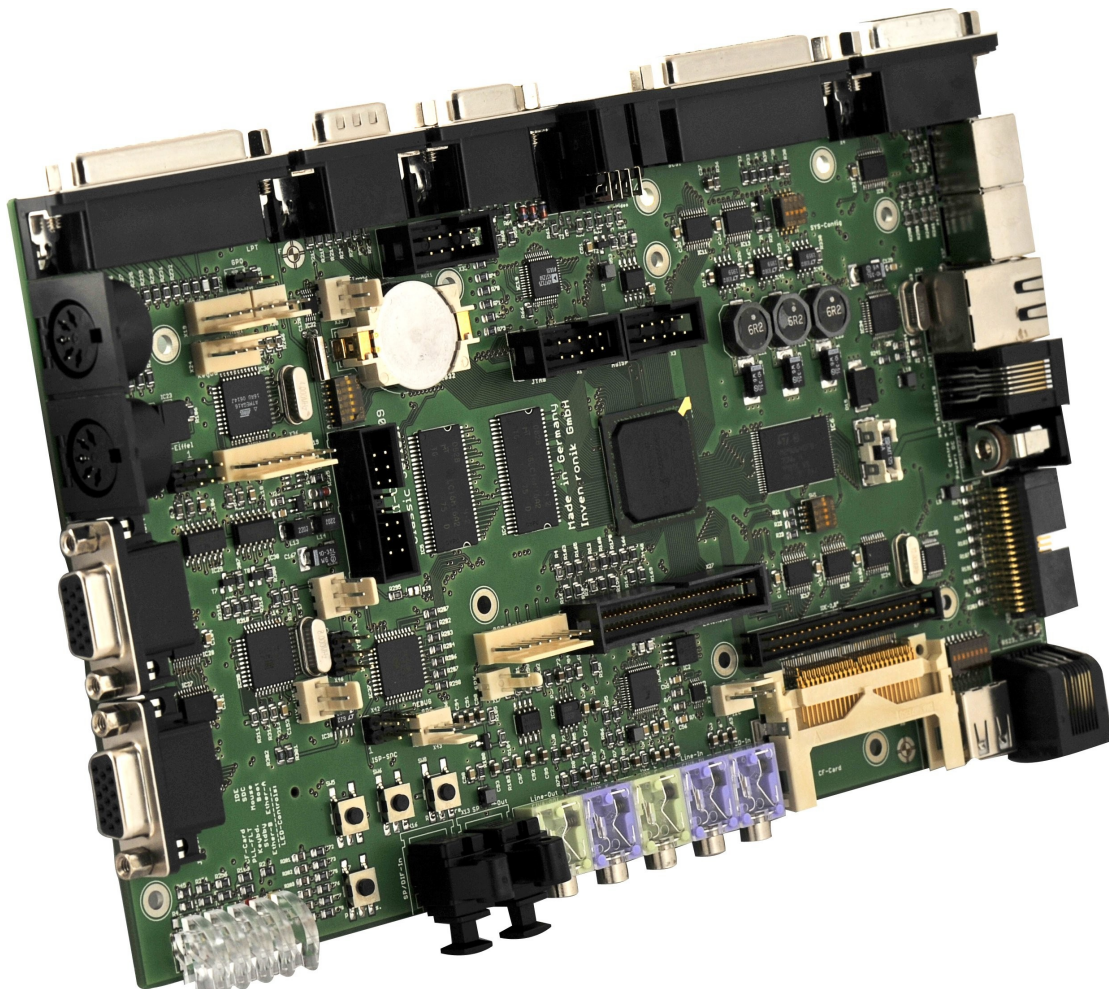


**Operating Manual for the Suska-III-C Hardware
as Target for the Realization
of Retro-Computers**



Have Fun!

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Inventronik GmbH 2009

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Introduction:

Suska-III-C is a universal digital electronic device based on a Cyclone-II FPGA (Field Programmable Gate Array) manufactured by the Altera corporation. The device type is EP2C35F484 (1). The FPGA can be understood as a universal configurable digital electronic device and is therefore the heart of Suska-III-C. The board is reconfigurable hardware that allows, in principle the creation of electronic devices with very different features. In particular the Suska-III-C board was developed as an Atari



Figure 1: The heart of the Suska-III-C: Cyclone-II FPGA device

ST/STE compatible computer. All interfaces of the original Atari machines are available on the Suska-III-C and there are interfaces foreseen to allow the use of modern peripheral devices such as USB or CF card memory. The following presentation is made with respect to the use of this hardware as an Atari ST/STE compatible computer.

In it's current version of the Suska-III-C IP core, the operating systems TOS1.00, TOS1.04, TOS1.62, TOS2.05, TOS2.06 and emuTos are tested and working. TOS1.02 is not working due to the high processing speed of the IP core. As shown in 2 the complete electronic design consists of the FPGA device in the middle of the picture, of the SDRAM left to the FPGA, of the operating system Flash device to the right of the FPGA, some other electronic devices and last but not least a high number of interface connectors.

The philosophy behind Suska is to realize electronic modules or functions inside the FPGA wherever it is possible. To do this, the parts of the electronic circuits are described abstractly using an appropriate standard language. The complete Suska project, means all logic modules is written VHDL (Very High Speed integrated Circuits Hardware Description Language). These descriptions, roughly speaking are translated by a compiler to a configuration file which, once downloaded to the FPGA, provides the functionality. Nearly all parts of the Atari ST or STE computers are provided as open source descriptions; named IP cores, where IP stands for Intellectual Property. The most recent version are available for download at www.experiments.de.

Functions which could not be realized in the FPGA, like digital analog conversion, the audio codec, the system memory, analog devices or the power management are equipped as discrete integrated circuits on the Suska-III-C board.

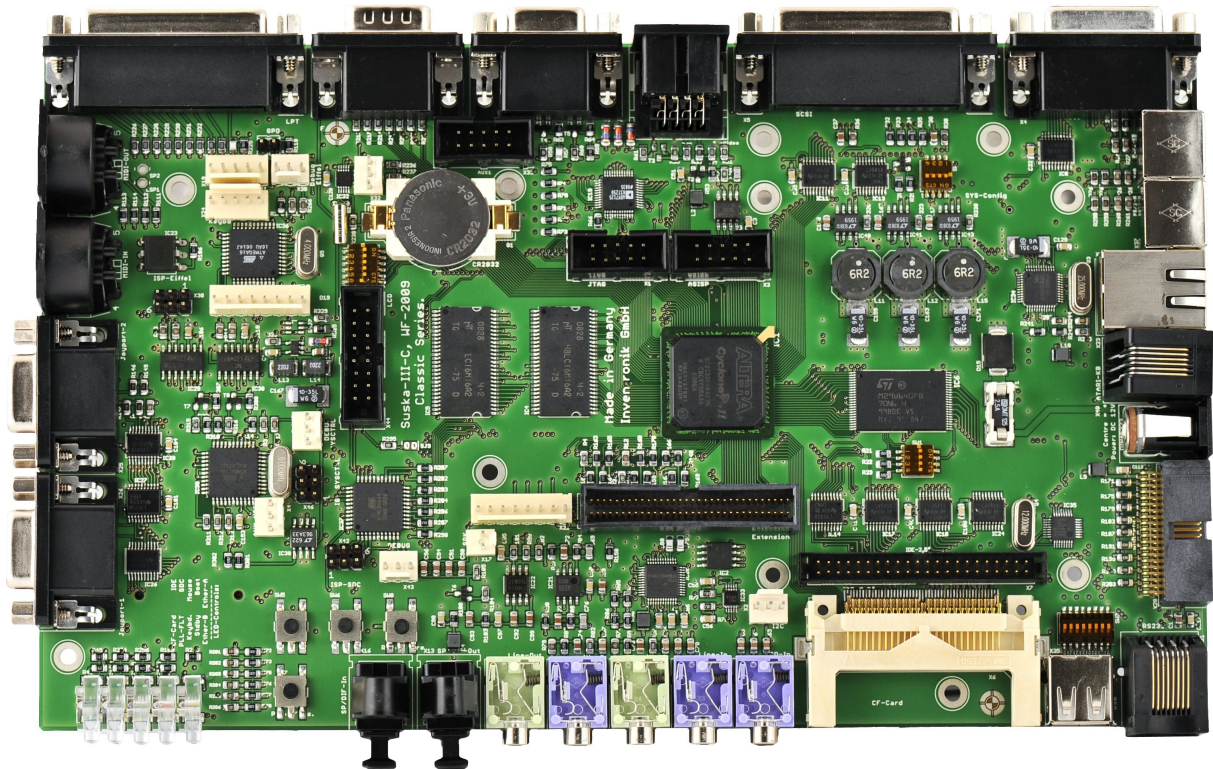


Figure 2: Suska-III-C Printed Circuit Board (Prototype with small Differences to the Series)

Suska-III-C also features a very low power consumption and has excellent operation using rechargeable batteries. All different operation voltages are provided on board from a single 7VDC to 12VDC supply. The three main power supplies are located on the right hand of the FPGA above the Flash device a shown in 2. The hardware is an 8 layer printed circuit board with a form factor of 234 * 140 mm². The overall height is given by the original Atari SST monitor plug and measures 27mm.

Besides the Atari ST/STE computers it is possible to implement other applications like Amiga relevant computer clones, as an example. The final decision regarding the FPGA and it's interfaces was made with an eye to creating the most flexible hardware possible. A clear difference between Suska-III-C and the majority of FPGA development boards available on the market today.

Equipping Suska-III-C with a slim operating system (MINT) to highlight a trend in the interaction between hardware and software is under consideration. Thanks to a large variety of interfaces, the board would then be suitable for a huge number of control applications.

Important Notice

The Suska-III-C hardware is intended for a power supply voltage of 7VDC to 12VDC. Please use only power supplies suitable for this application and with the necessary approvals. Do not exceed the absolute parameters for the operating voltage; please refer to the 'Technical Data'. Please avoid a reverse polarity. For more information on this refer to paragraph.

On the 8 layer printed circuit boards are devices with small dimensions and filigree structures. Please take absolute care not to apply mechanical stress to the printed circuit board for example by bending, torsion or strong forces to any connectors. Not respecting this point can lead to irreparable contact failures of the FPGA.

Take care when inserting programmer cables to the connectors on the top of the printed circuit boards. It is recommended to support the respective connectors on the solder side of the PCB to avoid mechanical stress.

Please be sure to use the printed circuit board (without a case) on an isolated surface and remove small particles like tin, wires or paper clips which could lead to short circuits.

Concerning this Documentation

The system's properties as described in this documentation depend on the implementation of the hardware in the FPGA. Because the model of the hardware is open source, the following description does not claim a fault-free system.

Error corrections and enhancements of the functionality are available through a simple update of the FPGA configuration. Especially when there is active development with numerous updates of the FPGA, it is possible that the system is running more or less stable depending on the success of the compilation and the fitting process. The reason for such instabilities is the timing behavior of the FPGA implementation itself. The printed circuit board and not responsible for such effects.

The manufacturer of the Suska-III-C hardware will not give a guarantee for any compilations of IP cores. Inventronik GmbH seeks to provide stable IP core updates in form of configuration files.

Initial Operation of the System

To operate the Suska-III-C hardware, there are some prerequisites necessary as described in the following paragraphs. The description given is a required minimum.

The Power Supply

Suska-III-C is operated from a power supply of 7VDC bis 12VDC. Use for example a wall cube adapter with a current of about 1.5A. Connect it to the power supply plug on the right-hand of the printed circuit board 3. The positive terminal is the center pin of the power supply connector.

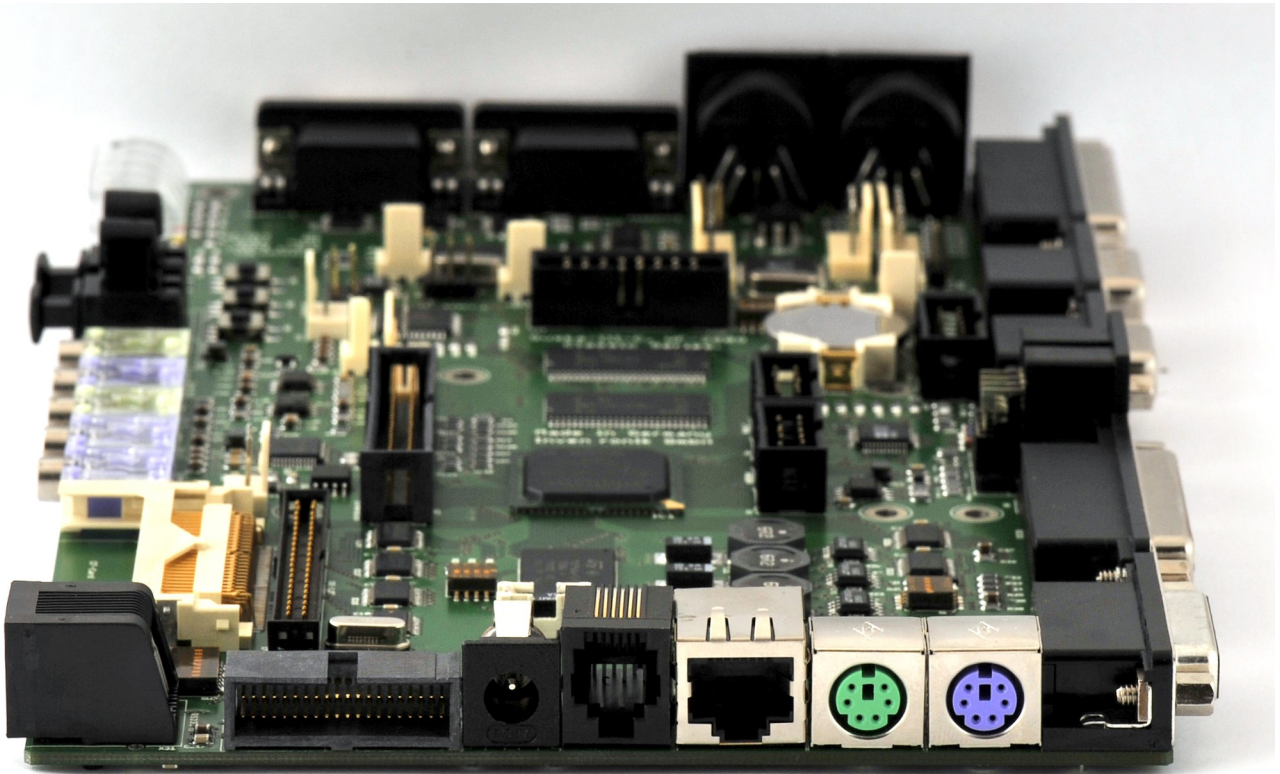


Figure 3: Right Hand Side of Suska-III-C with the DC Plug (left to the center).

Suska-III-C is protected against reverse polarity. This can lead to a melted fuse F1 (2,5AT) on the PCB. Replace this if required against an identical type (Shurter OMT 2,5A/125V).

Connection of the minimal required Peripheral Devices

To use the Suska-III-C hardware as Atari STE compatible computer clone it is required to connect a keyboard, a monitor and, where appropriate, a floppy disk drive.

The choice for the keyboard is either an original Mega STE or Mega ST type or a PS/2 version. It is not possible to use both keyboards at the same time. The keyboard is connected to its respective interface, for the original Atari keyboards this is the Western type connector right to the power supply and for the keyboard it is the purple PS/2 type connector. Also for the monitors there are different choices: Either original Atari monitors SM124, SC1225 or others which are connected to the original 13 position connector in the middle of the back side of the PCB or on the other hand VGA compatible monitors or TFTs connected to the VGA besides the Atari monitor connector (see 4).

Please be aware, that the support for the original monitors is given in any case. Due to the very limited availability of the Atari monitor connectors and the optional mounting of the 13 position Atari plug it might be necessary to equip the Suska-III-C PCB later with such a device. Satisfactory use of VGA compatible monitors or TFTs, will depend on the frequencies the monitor can handle.

The Suska-III-C IP core is already equipped with additional video modes capable of driving TFTs or CRTs. Further enhancements will be available by configware updates.

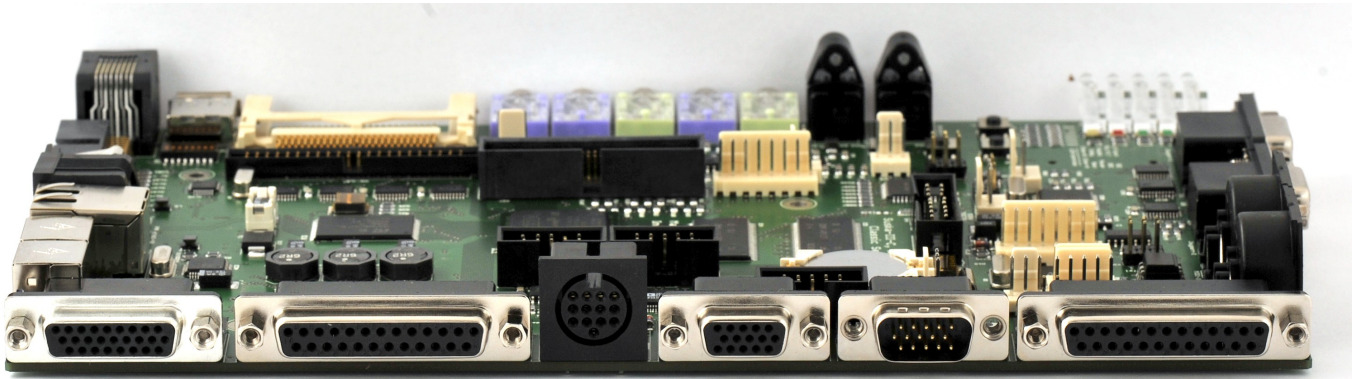


Figure 4: Backside of Suska-III-C, the original Monitor Plug is optional.

The floppy disk drive is connected via a 'high density' D-SUB connector with Suska-III-C. It is the second connector to the right as shown in 4. The terminal assignment of the connector cable is given in the appendix of this documentation.

System Configuration

Because the complete Atari compatible IP core is realized in the FPGA, enhancements beyond the original functionality are easy. To preserve the compatibility and to activate or deactivate special features, it is possible to configure switches or solder pads on the printed circuit board.

The switches are used for system configurations which may change from time-to-time. The solder pads are for configuration of features which accompany different versions of micro controller firmware or FPGA configurations and are changed only once or seldom.

Attention: switch off the Suska-III-C and disconnect it from the power supply to open or close the solder pads.

Configuration Switch FLASH_OFFSET (SW1)

The Flash device used on the Suska-III-C hardware has 64MBit of free memory, which are arranged in 4MWords₁₆. While the lower 524288 Words₁₆ are addressable by the FPGA, The upper address lines A19 to A21 of the Flash device are connected to the configuration switch (switch position 2 to 4). The switch position 1 of SW1 is not used, see 5, (on the right hand of the picture, there is located the 'Shurter' fuse F1). In this way, the different switch positions locate special address ranges as given in the following table.

Switch 2	Switch 3	Switch 4	Address Offset
Off	Off	Off	0x000000
Off	Off	On	0x080000
Off	On	Off	0x100000
Off	On	On	0x180000
On	Off	Off	0x200000
On	Off	On	0x280000
On	On	Off	0x300000
On	On	On	0x380000

Table 1: Address Offsets of the Flash Memory

A practical application of this feature is the selection of different operating systems which are located at the respective address boundaries. For more information refer to the paragraphs Loading the Operating System via the Bootloader Mechanism or Loading the Operating System via SD Card .

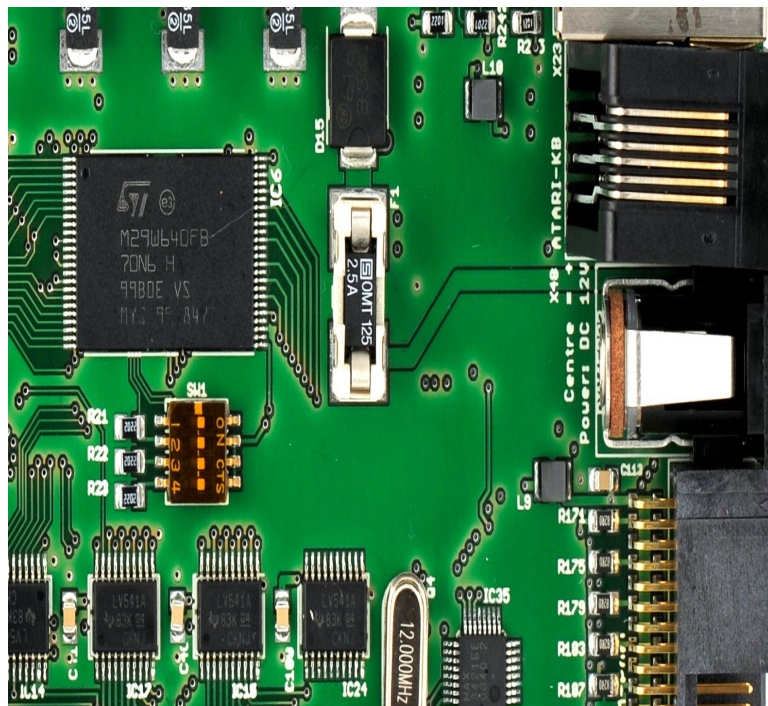


Figure 5: Flash Memory with Configuration Switch SW1.

Configuration Switch SCSI_ID (SW2)

SW2 has 4 Switches. The SCSI-ID of the SCSI host controller is selectable by the switches 1 to 3. The arrangement is chosen in a way resulting in a binary representation. An example: 1=On, 2=Off, 3=Off refers to the SCSI-ID 4.

Switch number 4 is intended to switch the PS/2 functionality. Refer to the paragraph The PS/2 Micro Controller for more information.

The position of the switch is given in 6.

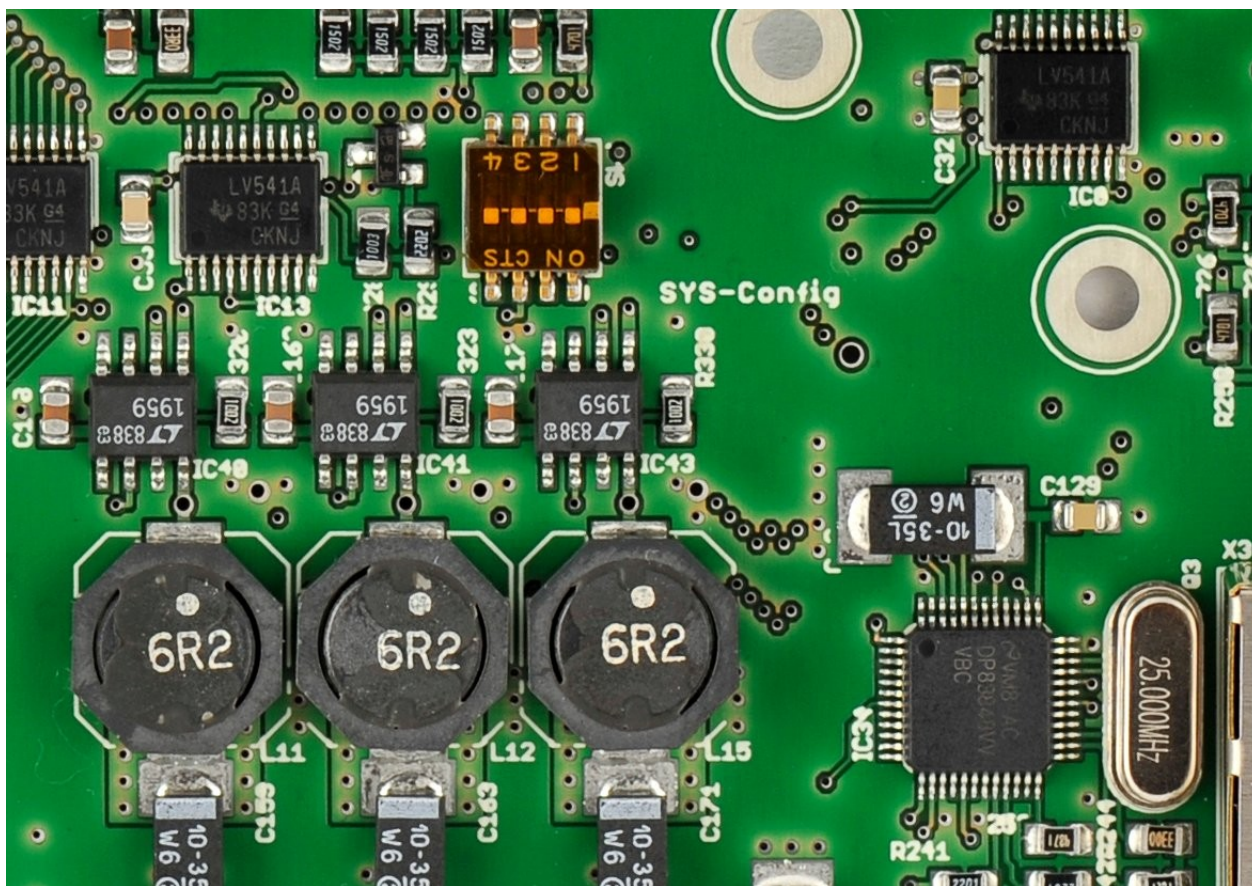


Figure 6: Configuration Switch SW2 "SCSI-ID"

Configuration Switch MST_Config (SW3)

The function of SW3 is identical to the 8 position switch which can be found in original Mega STs and is intended for general system configuration. Because of the high degree of freedom concerning the development of the Suska-III-C IP core in conjunction with the FPGA and the resulting numerous 'selection free' improvements over the original machines, currently this switch is mostly not used. It is intended for future use.

One exception exists for newer TOS versions which use the switch number 7 to indicate whether DD or HD floppy disk drives are used. If 'on' the operating system handles HD-floppy disk drives otherwise DD types. One can see this in the dialog box of the formatting routine which shows the additional entry 'High Density' when HD drives are selected.

The IP core is in this point an improvement over the original hardware. The HD information is not indicated to the floppy drive but indicated by the floppy drive. So setting switch number 7 is less important. Formatting floppies can sometimes lead to better results when used in conjunction with the option 'High Density' for HD type floppies thanks a better selection of stepping rates for the drives provided by the operating system depending on the setting on switch 7. HD type floppies which are formatted without the option 'High Density' show 726K of free disk space. This is a faulty information. HD type floppies always have a capacity of 1,44MB after formatting. More information concerning the configuration switch SW3 can be found in the Appendix 3: Mega STE Configuration Switch.

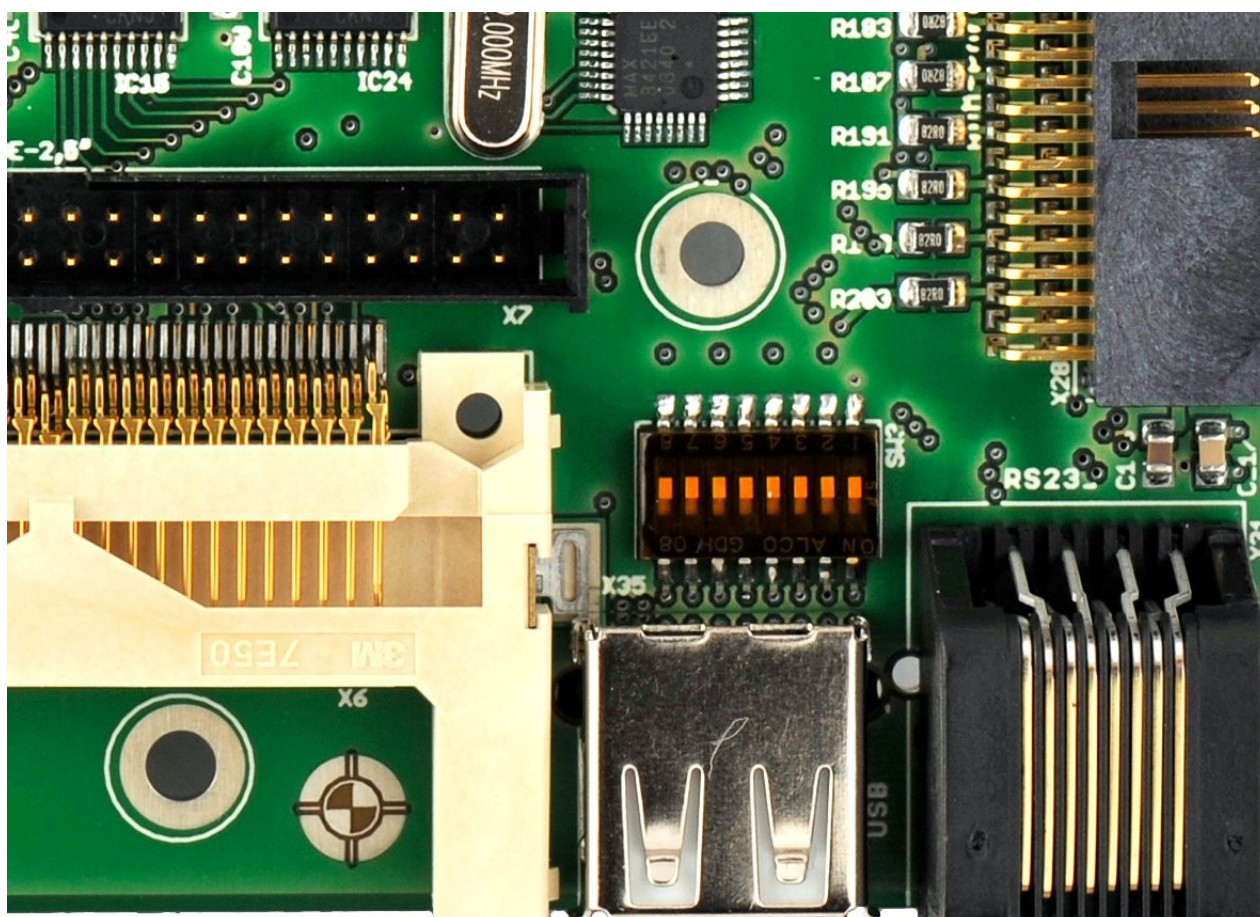


Figure 7: Configuration Switch SW3 – (Meets the switch of the Mega STEs).

Configuration Switch SYS-Config (SW4)

This switch provides six selection switches which are used by the Suska-III-C IP core as follows (for more information

refer to the IP core source code):

Switch 1:

Selects the system speed. While original STs are driven with a CPU clock of 8MHz, the Suska-III-C IP core is driven with a CPU clock of 16MHz. This is necessary to provide the correct video bandwidth for multi-sync monitors. The high frequency leads to incompatibilities with software which for example implements time delays in NOP loops. Also affected are the old TOS versions 1.00, 1.02 and 1.04. Setting this switch to '1' reduces the CPU speed resulting in better compatibility (unfortunately not 100%).

Switches 2 and 3:

These two switches are intended to select enhanced video modes. Depending on the connected monitor type the selection are for example 'legacy mode' for the original Atari monitors (both switches off), the multi-sync modes and the multi-sync monochrome mode (both switches on). Play around with the settings to find the best result.

Switch 4:

This switch selects the available memory used by the IP core. 'Off' means 4MB memory like in STs or STEs and 'On' means 14MB memory used in the Falcon.

Switch 5:

For the compatibility to original ST(E) machines, the setting ACSI interface active must be selected (switch is off). If the switch is in position 'ON', ACSI is deactivated and the ACSI to SCSI conversion via the ACSI to SCSI bridge is active. In this case, the SCSI interface is in operation. Since the IP-Core version 2K13A this switch is not used anymore. The ACSI and the SCSI interface can now be used simultaneously.

Switch 6:

This switch selects the base address for the operating system. Switched off, the base address is 0x00FCxxxx and therefore suitable for the operating systems TOS 1.00 bis TOS 1.04. For TOS1.62, TOS 2.05, TOS 2.06 and emuTos the base address 0x00E0xxxx must be selected by switching S6 on.

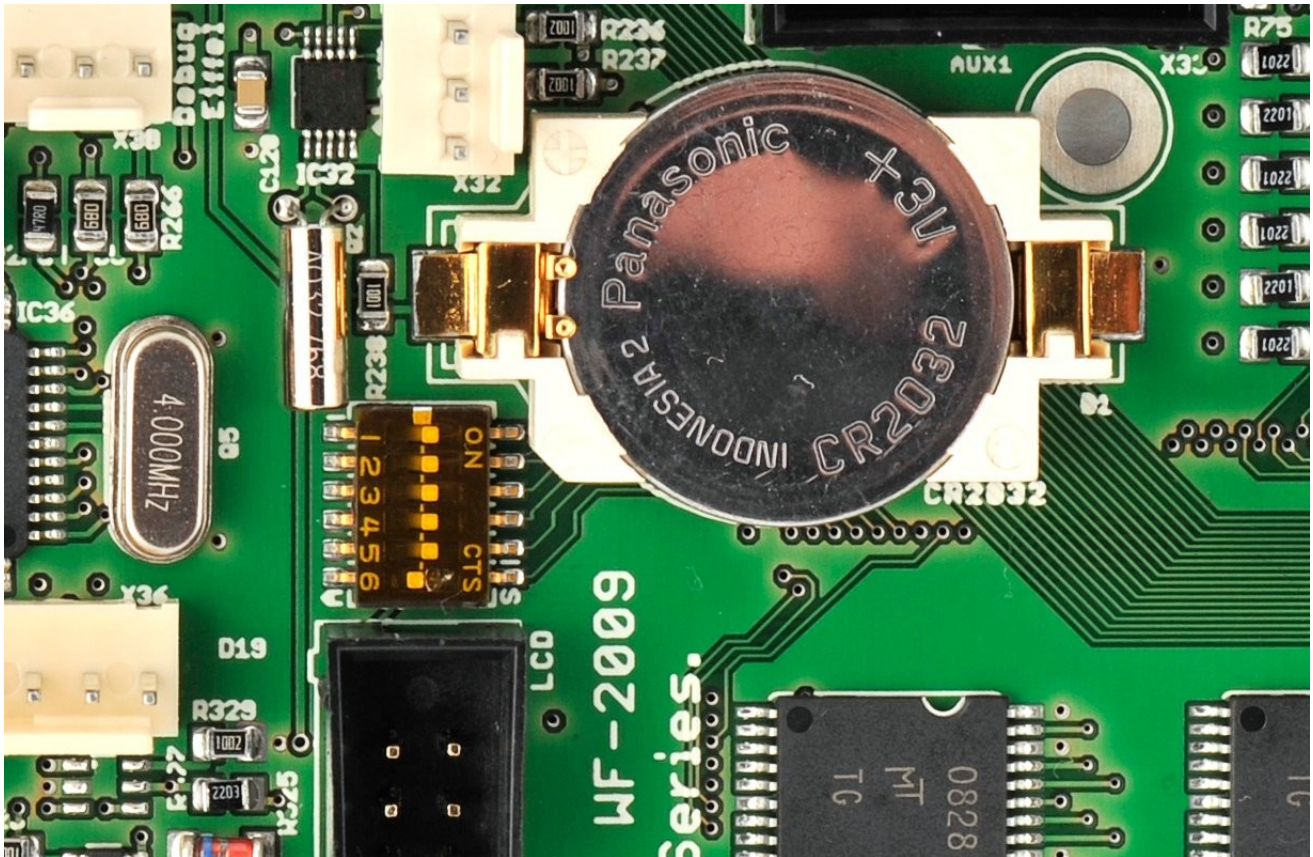


Figure 8: Selection Switch for general System Settings

Solder Pads SJ1 and SJ2

The MIDI interface is connected to a 6850 compatible ACIA (**A**synchronous **C**ommunication **I**nterface **A**dapter) which is implemented as IP core in the FPGA. It has inputs for the Clear To Send (CTS_n) and the Data Carrier Detect (DCD_n) Signals. These are not used in original ST machines and therefore connected to GND. Opening these solder pads gives the freedom to introduce enhancements to the IP core or operating systems which use these signals.

The two solder pads are closed by default see 9. The exact location of these solder pads can be taken from the layout of the solder side of the printed circuit board in the appendix.

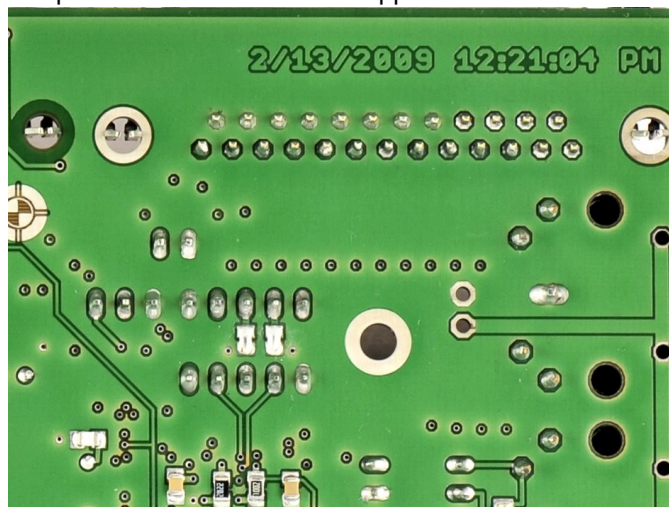


Figure 9: Solder Pads SJ1 and SJ2 on the PCB's Solder Side.

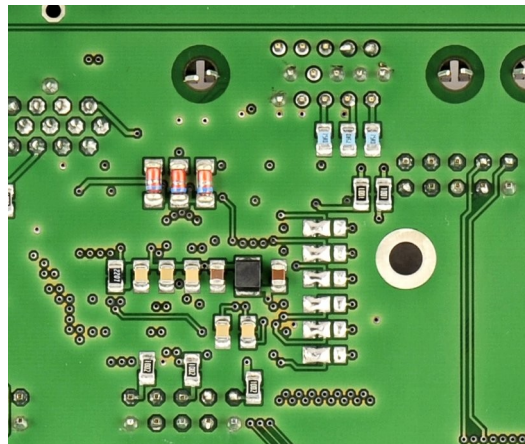
Solder Pads SJ3 to SJ8

The color graphic modes of the STEs allow a maximum of 4 bits per color. The Suska-III-C hardware uses a video AD converter with 8 bits per color. The two least significant bits D1 and D0 are connected to GND for each color and the respective four most significant bits D7 to D4 are connected to the graphics controller of the Suska-III-C IP core.

The bits D3 and D2 can be connected via the solder pads alternatively. Connected to GND results in a color resolution like in STE machines with 4 bits resulting in a maximum of 4096 different colors. Connected to XFF827E_D7 to XFF827E_D2, coming from the FPGA, the color resolution is, in principle, 6 bits resulting in 262144 different colors.

To use this feature, it is necessary that the IP core provide enhanced video mode and the signals XFF827E_D7 to XFF827E_D2, which refer to the respective ST-Book register are not available outside the FPGA. See also the wiring of IC39 (system micro controller), X33 (Aux2 connector) and IC37 (SD card micro controller). 10 Shows the location of the solder pads. The detailed notation can be taken from the layout of the solder side of the printed circuit board in the appendix.

Figure 10: Solder Pads SJ3 to SJ8 on the



PCB's Solder Side

The solder pads are all connected in position 1-2 by default.

Solder Pad SJ9

The SD card micro controller (IC37) is intended primarily for programming the FPGA boot device or copying an operating system image to the Flash memory. In its non-configured condition the FPGA provides no functionality so the SD card micro controller must be driven with the 4MHz clock on the PS/2 micro controller as this does not rely on the FPGA.

Once the FPGA is correctly configured, the signal SDC_AVR_CLK can be connected to the SD card micro controller by clocking SJ9. In this way any desired clock frequency can be used for IC37. The clock functionality for SDC_AVR_CLK must be provided by an appropriate IP core module.

The FPGA I/O pads are high impedant in the case of a non-configured device, so the SD card micro controller can be driven with the 4MHz PS/2 micro controller clock, even if SJ9 is closed. In that case, the clock comes from the SD card micro controller via the resistor R295. If the clock comes from the FPGA, the driver strength of the respective I/O pads on the FPGA is sufficient to drive the clock against R295. In the case of a malfunction of SDC_AVR_CLK, it is not possible to reconfigure the FPGA's boot device from the SD card micro controller because the clock is missing. A workaround is to open SJ9 or to configure the FPGA via the Active Serial Interface using a programmer.

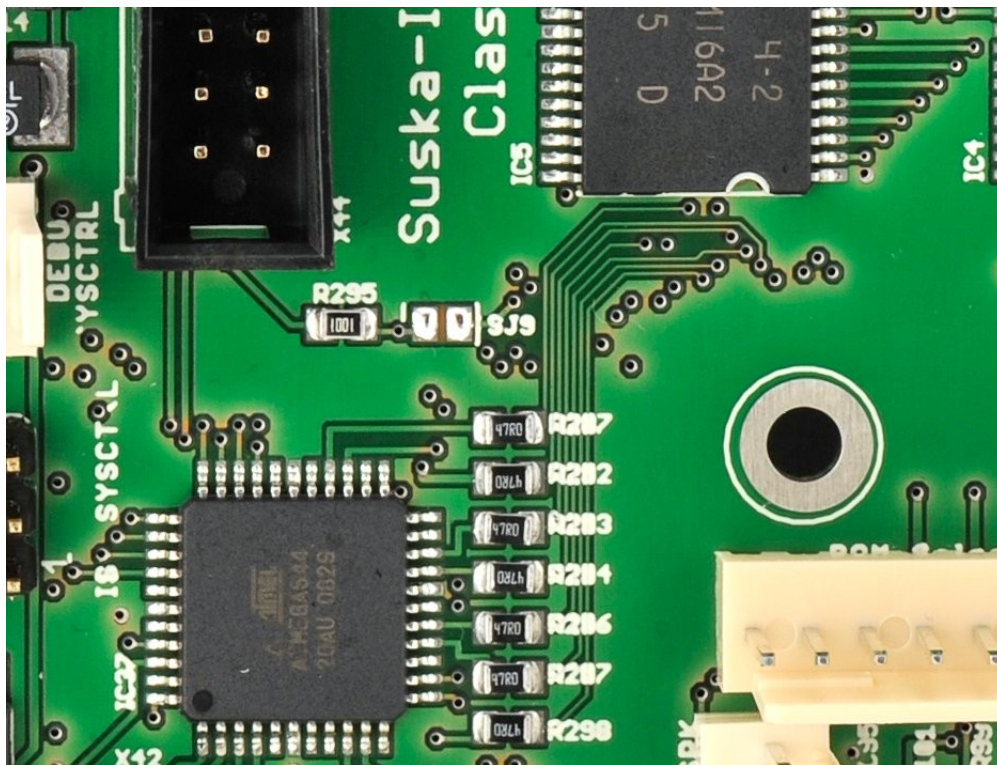


Figure 11: Solder Pad SJ9 on the PCB's Top Side.

The solder pad SJ9 is open by default.

Description of the System

The System Micro Controller

Suska-III-C is equipped with a system controller which tracks operating condition and power consumption. This functions are implemented in the system micro controller IC39 in 12, which is operated from a standby power supply. One of it's tasks is to supervise the reset buttons (see also the paragraph concerning system reset), to switch the different power supplies of Suska-III-C, and to load the various operating systems via a boot loader mechanism.

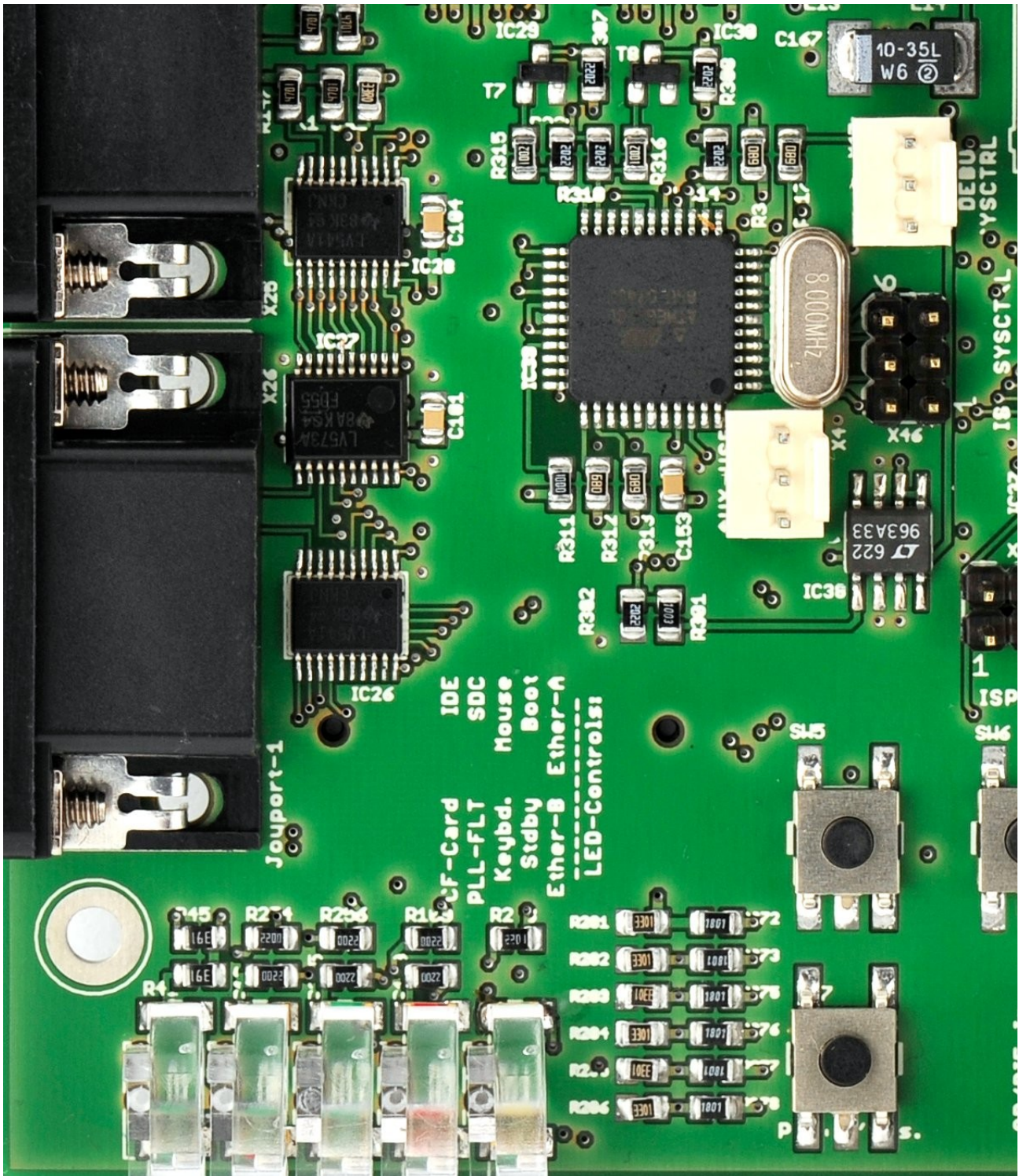


Figure 12: The System Micro Controller.

from a PC to the Flash memory. A detailed description of this feature can be found in the paragraph Loading the

Operating System via the Bootloader Mechanism.

Between IC39 and the FPGA there are several signals intended for future use. More information can be found in the schematics of Suska-III-C. This micro controller is additionally equipped with an interface Aux-USB (X45). It can for example be used to communicate with USB devices if the micro controller software supports this functionality. IC39 is programmed via the interface ISP_SYSCTRL (X46) and has the option to output debugging information via the interface SYSCTRL_DEBUG (X47).

For programming the micro controller and exchanging debugging information there are appropriate protocol adapters available. Detailed information concerning the programming are described in paragraph Programming Firmware to the Micro Controllers. For more information concerning the protocol adapters refer to the user manuals of each respective product.

The PS/2 Micro Controller

A second micro controller (IC36) provides the functionality of a keyboard controller. It is not provided in the IP core because it was a built-in component of original ST(E) or Mega ST(E) keyboards. This controller detects PS/2 keyboards and mice and provides the correct information for the ACIA IP-Core in the FPGA, and allows a protocol compatible to original Atari keyboards. In this way, PS/2 devices can be used without changes to software or operating system.

Because modern keyboards have a little bit different layout as Atari devices, there arose the need to translate a few keys. A table in the Appendix gives information about these changes.

Use of PS/2 keyboard and mouse does result in the lack of the mouse and joystick connectors. The mouse is replaced and no problem, but additional hardware is still necessary for a joystick to be connected. A bridge adapter to handle the translation of the joystick information is available from Inventonik GmbH and can easily be connected through the AUX3 interface (X36) of the PS/2 micro controller.

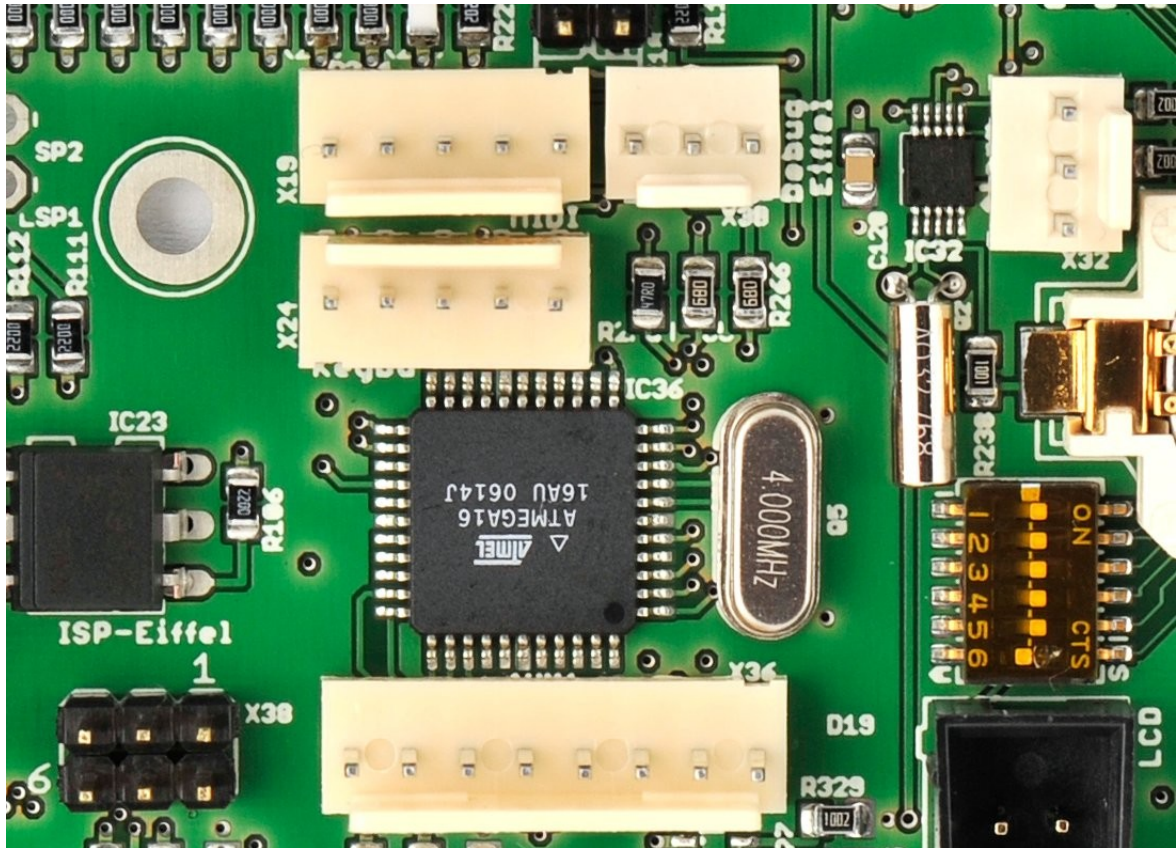


Figure 13: Der PS2 Micro Controller.

The two buttons SW5 and SW6 are connected to the port pins PD6 and PD7 of IC36. They are intended for general future enhancements and require changes to the software of the PS/2 micro controller and possibly to the Suska-III-C IP core.

The port pins PC4 and PC5 are connected to the two LEDs 'Keyboard' and 'Mouse' and allow a signaling of the shift lock key and the detection of a mouse. IC36 is configured by connecting a programmer to the interface ISP_PS2 (X38) and has a debugging interface PS2_DEBUG (X39).

For programming of the micro controller and the exchange of the debugging information there are appropriate protocol adapters available. Detailed information concerning the programming are described in paragraph Programming Firmware to the Micro Controllers. For more information concerning the protocol adapters refer to the user manuals of the respective products.

The switch 4 of the SCSI_ID (SW2) configuration switch is currently not used. Originally it was intended to enable the PS/2 functionality. Using an 'intelligent' micro controller software makes the use of this switch unnecessary. Hence the switch is useful for general purpose use involved with enhancements of the micro controller firmware.

The SD Card Micro Controller

The SD card micro controller (IC37) provides the communication between the FPGA and SD cards (X41). Primarily this controller is used to copy operating system images to the Flash memory or to update the FPGA's boot device. It is required, that the image files are located on the SD card. This functionality is intended for a simple maintenance of Suska-III-C without the need of a programming adapter.

The enhancements of the IP core and the software of the SD card micro controller are in progress and will probably be released with the next version of the Suska-III-C IP core.

PB0 if IC37 is capable of driving the LED 'SDC', which signals communication with the SD card. IC37 is programmed via the interface ISP_SDC (X42) and has a debugging interface SDC_DEBUG (X43).

For programming of the micro controller and the exchange of the debugging information there are appropriate protocol adapters available. Detailed information concerning the programming are described in paragraph Programming Firmware to the Micro Controllers. For more informations concerning the protocol adapters refer to the user manuals of the respective products.

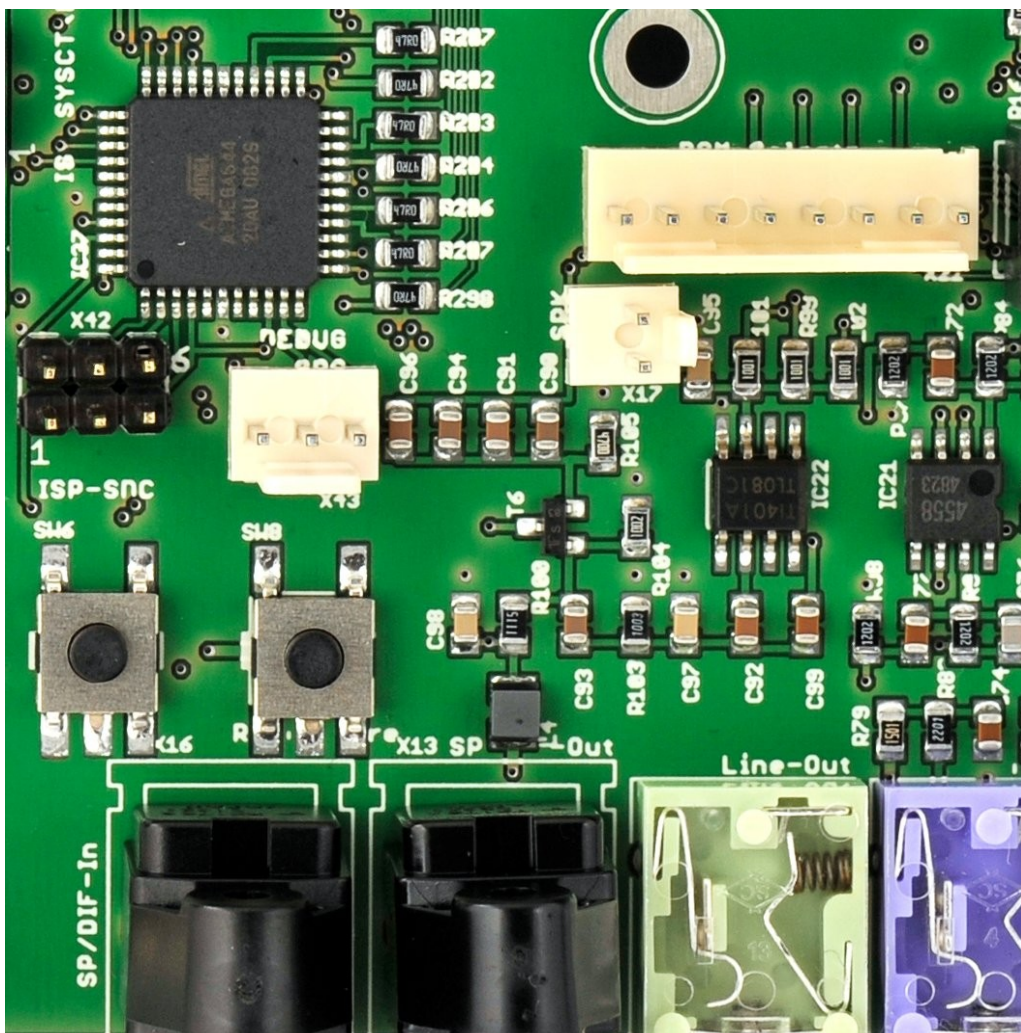


Figure 14: The SD Card Micro Controller.

The Field Programmable Gate Array (FPGA)

The Suska-III-C hardware comes with an Altera FPGA. It is a Cyclone II, type EP2C35F484 in a 484 pos. ball grid

case. This device is responsible for providing the main functionality of the Atari compatible Suska board. The IP core featuring a STE machine uses about 20.000 of the total available 35.000 logic elements of the FPGA. So there is enough space in the chip for further enhancements. The digital logic, implemented in the FPGA can be changed by reconfiguration of the IP core. For more information refer to the paragraph Loading the FPGA IP-Core.

IP-Core in the FPGA

The Suska IP core ist completely written in VHDL (**V**ery **H**igh **S**peed **I**ntegrated **C**ircuits **H**ardware **D**escription **L**anguage), as this language is best suited for the abstract modeling of digital circuits. The syntax of VHDL is very detailed and self-explanatory. The core is in mostly available under the LGPL open source license and can be downloaded from <http://www.experiment-s.de> .

The design software Quartus can be used for enhancements and changes of the IP core. Quartus is available as subscription version and also as a free web edition version. The software contains all the necessary modules: compiler, fitter, simulator, programmer etc. The current Suska IP core version is 2K9A and features the following hardware modules:

- 68000 compatible CPU module.
- Atari Blitter compatible graphics processor.
- Atari GLUE (mixed logic) compatible logic module.
- Atari MCU (**M**emory **C**ontrol **U**nit) compatible logic module.
- Atari DMA (**D**irect **M**emory **A**ccess) compatible logic module.
- Atari Shifter (video processing) compatible logic module.
- Atari Shadow (LCD controller) compatible logic module.
- WD1772 compatible floppy disk controller module.
- MFP68901 compatible multi function port module.
- YM2109 compatible sound chip module.
- 6850 compatible ACIA (**A**synchronous **C**ommunication **I**nterface **A**dapter).
- Several interface adapters (IDE, ACSI, SCSI).
- Bootloader module.

The various modules are wired together in a so called top level design. The modeling is done such that the wiring, the signal names, the module arrangement and the module functionality as closely as possible match the original

hardware layout and schematics of the 1040ST or the 1040STE machines. It would far exceed the scope of this document to describe the IP core in detail and due to the high development speed of the core and the resulting changes, it is recommended to use the Suska-III-IP core sources and related documentation for more detailed information.

Ethernet Device DP83848C

With the Ethernet controller DP83848C Suska-III-C is equipped with a commonly used 'physical layer' device capable of handling transfer rates of 10/100 Mbps. There is a data sheet for this integrated circuit containing a lot of information how to use and program it. The controller is directly connected to the FPGA and can be used if the Suska-III-IP core is enhanced with an appropriate interface and if the drivers for the operating system are available.

USB Controller MAX3421E

The MAX3421E is a USB host controller device, which is controllable over a SPI interface connected to the FPGA. Enhancements to the IP core and to the system software and/or the operating system are required to operate this device. The controller fulfills the USB specification rev. 2.0. The maximum transfer rate of the SPI interface is 26MHz. This limits the maximum available data transfer rate over USB. Detailed information to this device is available in the respective data sheet.

Video DAC ADV7125KST50

With this device, which features three high speed 8 bit video DACs the Suska-III-C hardware is equipped with a quality video system never available with the original ST or STE machines. Although there are only 4 respective 6 bits per color, (see also the paragraph Solder Pads SJ3 to SJ8) in the current IP core version, the brilliance and dynamic of the video information exceeds by far the original ST hardware and gives the Suska-III-C an outstanding feature.

Audio-DAC AD5302

In the original STE machines there are two 8 bit DA converters for generating system sound. These DAC0802 types are driven by a parallel data bus and are not recommended for new designs. As a replacement, Suska-III-C is equipped with a small integrated circuit which contains two 8 bit DA converters that are driven over a SPI interface (Serial Peripheral Interface) of the type AD5302 resulting in a reduction of the 16 data lines required for the DAC0802 to only 3 signals required for the SPI driven with a frequency up to 30MHz. It is possible to generate the audio signals without any reduction in quality in comparison to original ST(E) machines.

The Suska IP-Core features a module for converting parallel audio data to the SPI protocol of the new DA converters. The outputs of the two DA converters are connected to the AUX inputs of the audio codec CS4299, so the volume and tone of the audio signal are controllable, a feature originally implemented in the obsolete and scarcely available LMC1992 in the ST(E)s.

Audio-Codec CS4299

As described above, the audio equipment in the original Atari STE machines is not up to date. Nowadays there are modern audio processors with built-in DA converters capable doing AD conversion. Furthermore these chips contain analog multiplexers, mixer demultiplexers and so on. Suska-III-C has such an electronic device of the type CS4299 to make the audio functionality much more comfortable than the STEs. The audio codec is controlled (like the AD5302) over a second SPI interface.

To use the CS4299, there are enhancements over the current Suska-III-C IP core necessary and appropriate drivers for the operating system or the software. The CS4299 is connected to the following inputs or outputs:

- AUX-Channel is connected to the audio DACs AD5302
- CD input
- Microphone input left
- Microphone input right
- Line input
- Line output
- SP/DIFF output (digital)

The data sheet of the CS4299 is detailed. Please refer to this for information concerning the electrical data and the programming of the device.

Further Audio Hardware

Suska-III-C is also furnished with some 1040ST relevant hardware, to provide one mono audio channel driven by the YM2149 compatible audio IP core. The audio signal is boosted by an operational amplifier (IC22) and is connected to the 'Speaker' connector (X17) and to the Atari monitor connector (X9) pos. 1. The counterpart to the SP/DIFF output there is a SP/DIFF input for digital audio transmission.

Real Time Clock DS1392

The RP5C15 real time clock used in the original STs and STEs is obsolete and has been replaced by the DS1392 (IC32). Unfortunately it is not register compatible to the RP5C15. To eliminate this disadvantage, the Suska-III-C IP core has a module which to widely manage compatibility and control the serial interface for data exchange between the FPGA and the DS1392. For information on the DS1392 registers refer to it's data sheet.

Pushbuttons and Operation Displays

Suska-III-C has four pushbuttons SW5 to SW8 and five double LEDs. In 15 the location of the pushbuttons is shown.

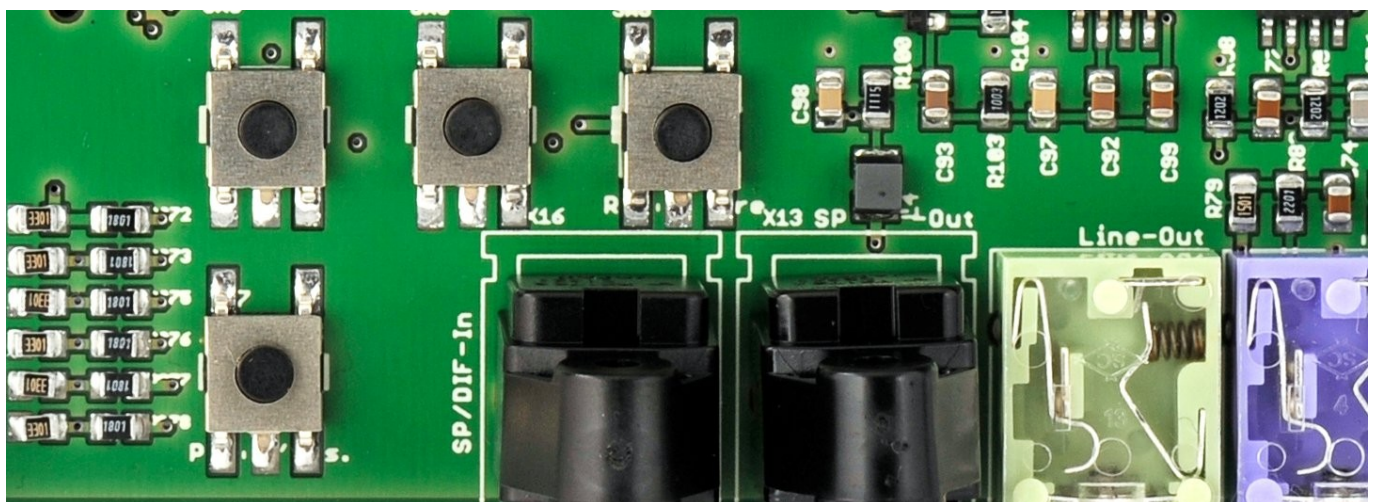


Figure 15: Pushbuttons of Suska-III-C.

SW5 and SW6 (upper left and upper middle) are intended for general future applications as for example the control of the contrast if a liquid crystal display is connected. The buttons are connected to the micro controller (IC36) which is responsible for management of the PS/2 devices. Functionality for the pushbuttons is done through an appropriate addition to the micro controller firmware and, if required, additions to the Suska-III-C IP core.

SW7 (lower left) is the power switch which also features the reset function for the system. A **short keystroke** to SW7 is sufficient to switch the system on. To switch it off, a keystroke of about three seconds is required. A short keystroke to SW7 (when the system is on), releases a system reset.

SW8 (upper right) is the reset button for the FPGA and is also used, with the help of the boot loader module implemented in the FPGA's logic, for loading operating systems in the Flash device. The boot loader mechanism is described in the paragraphs Loading the Operating System via the Bootloader Mechanism and Loading the Operating System via SD Card . During normal operation this pushbutton is not in use.

Die LEDs front view is shown in 16 (left side). The LEDs have the following meaning (1= lower left, 2 = upper left, 3 = lower second from the left and so on):

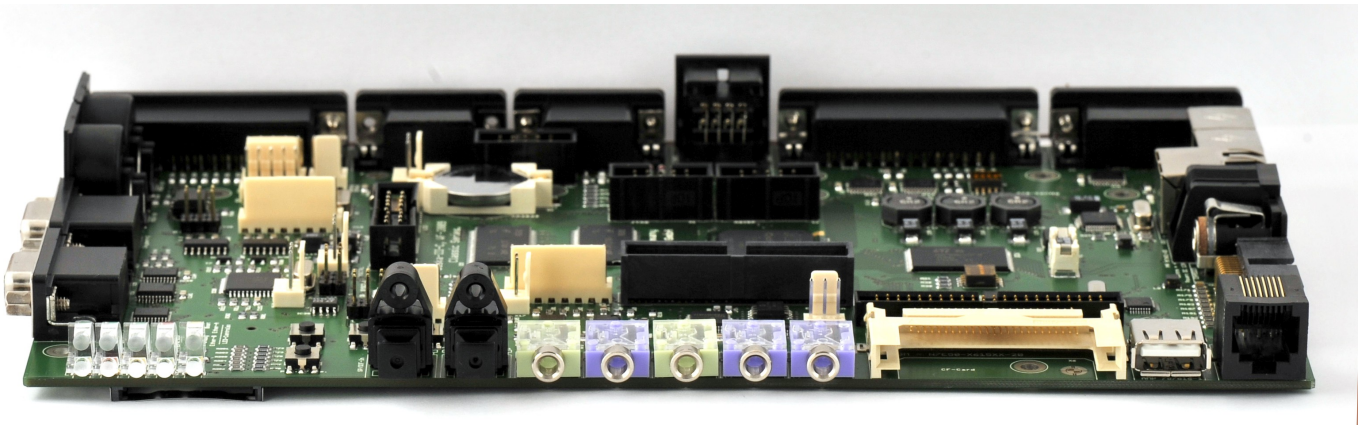


Figure 16: Front View of Suska-III-C.

1. Hard drive access of an installed CF card (Compact Flash).
2. Hard drive access of an installed 2,5" hard disk.
3. Error detection of the FPGA's phase locked loops. This LED indicates catastrophic system failure.
4. Hard drive access of an installed SD card.
5. Keyboard indicator: PS/2 keyboard shift lock status.
6. Mouse indicator: PS/2 mouse exists an a function is detected.
7. General operation indicator.
8. Bootloader LED. Refer to Loading the Operating System via the Bootloader Mechanism and Loading the Operating System via SD Card .
9. Ethernet is active.

10. Ethernet link.

Description of the Interfaces

Suska-III-C features a wide variety of interfaces. There are most ST- and STE as well as a couple of additional interfaces. The electrical data and the functionality of the different interfaces are well known and described in the respective literature, and a detailed description is not in the scope of this document. The peculiarities and the location of the interfaces on the Suska-III-C hardware is given in the following paragraphs.

Interfaces located at the Front

16 shows the interfaces located at the front side of the PCB. Each of these has in common that they are either not always connected, or they require easy accessibility. They include the digital SP/DIFF interfaces, the audio connectors, the SD card and CF card connectors, the USB port and the serial interface which is implemented by a RJ45 plug on the right-hand side. The terminal assignment of the serial plug is given in the appendix (pos 1. is to the left). If a CF card is used in IDE mode and if it is in cable select mode, this interface is configured slave.

Interfaces on the left Hand Side of the PCB

On the left-hand side are the MIDI interfaces and both STE compatible joy ports.

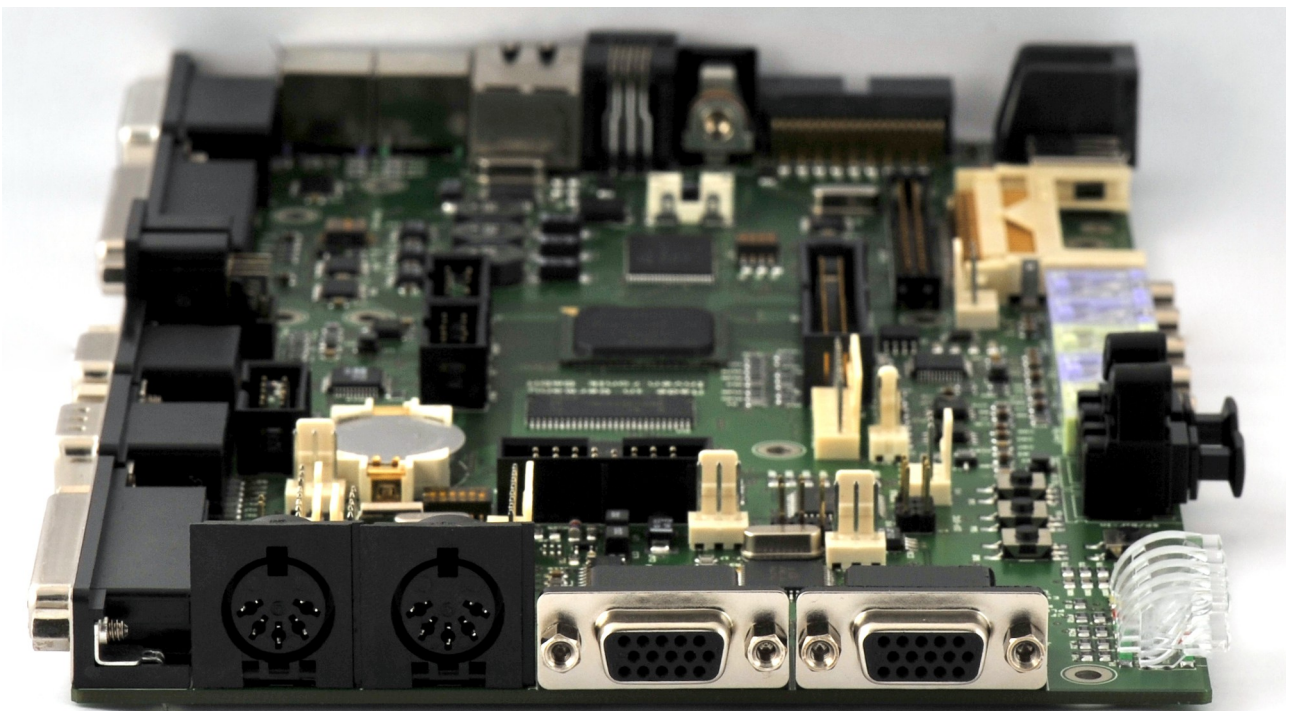


Figure 17: Suska-III-C View from the left.

Interfaces on the right Hand Side of the PCB

On the right there are: the ROM port, the power supply, connector for an Atari keyboard, Ethernet plug, PS/2 mouse (green) and keyboard (purple). The original ROM port connector is not available and is replaced by an industrial type. The terminal assignment for these connectors is found in the appendix.

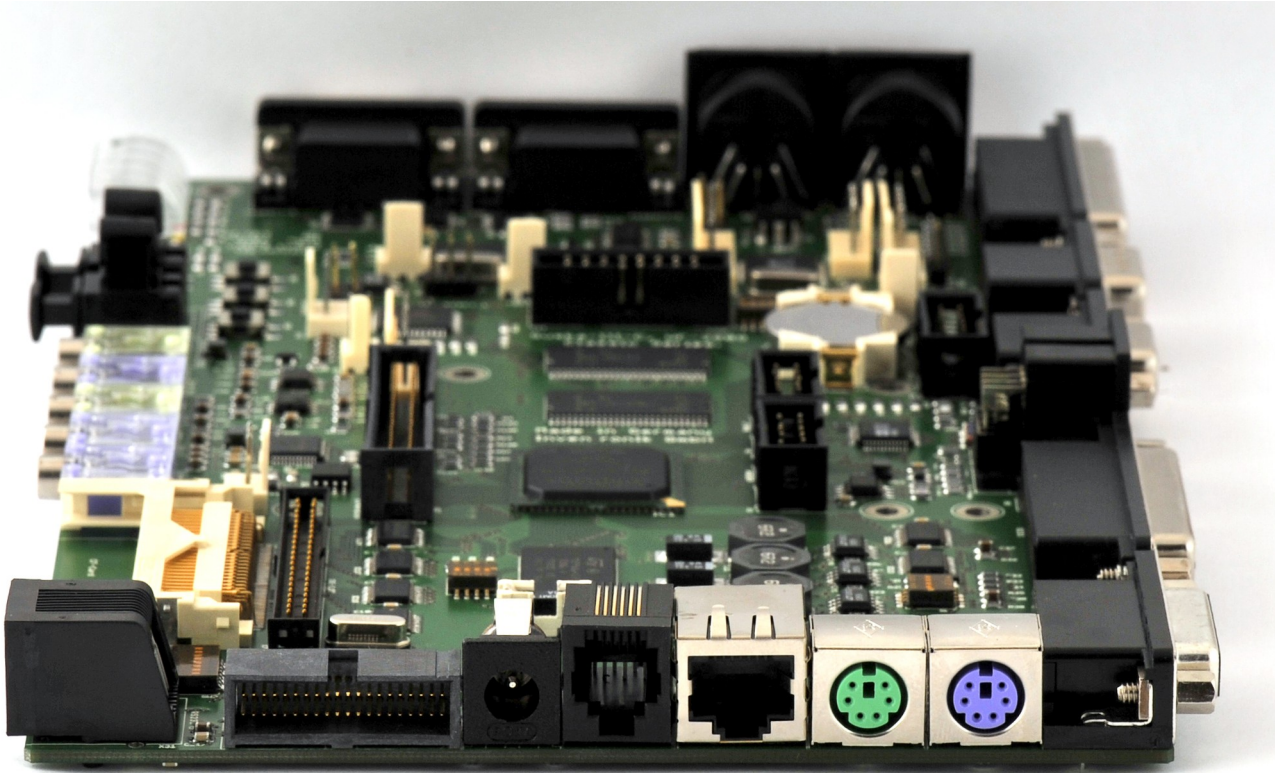


Figure 18: Suska-III-C View from the right.

Interfaces on the Back Side of the PCB

On the back side are the classic ACSI bus interface, the SCSI connector, the Atari monitor plug, the VGA monitor plug, the interface for the floppy disk drive and the printer port. The connector for the floppy disk drive is a HD type D-Sub with 15 positions. The terminal assignment for these connectors is found in the appendix.

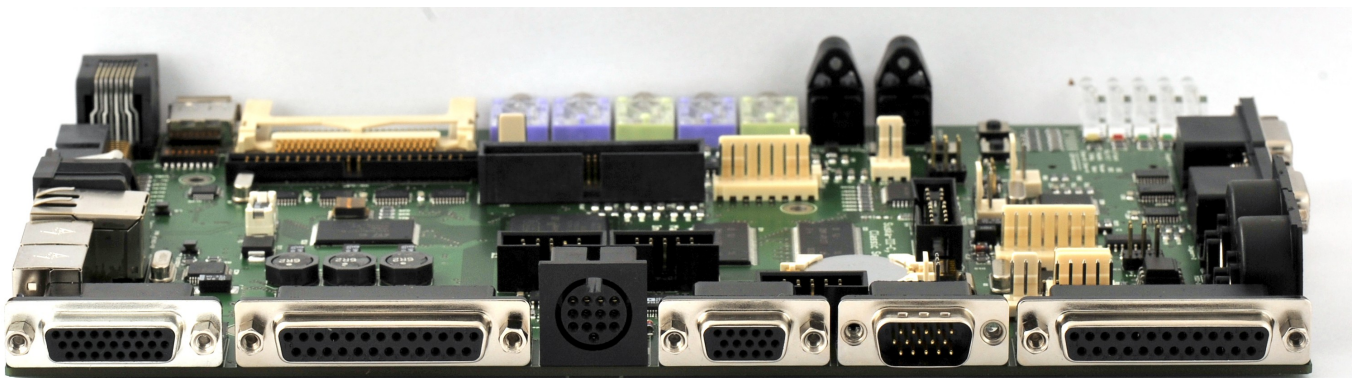


Figure 19: Suska-III-C View to the Back Side.

Peculiarities exist for the ACSI interface, which is not directly connected to the FPGA but to line drivers to provide level shifting between 3,3V and 5,0V and vice versa. The SCSI interface is realized in the same way and is also equipped with an electronic bus termination.

Interfaces on Top of the Board

There are a couple of other interfaces not described yet and which can be accessed from the top side of the PCB.

The terminal assignments and if necessary the connector types are given in the appendix of this document as is a layout of the top of the printed circuit board indicating the location of the connectors.

X7 is the IDE connector. It can be connected directly to 2,5" hard disk drives. Use a short cable as possible. When drives in cable select mode are used, this interface is configured master.

X17 is the connector for the speaker. The audio signal comes on the terminal located in direction to the center of the PCB. The other one is connected to GND.

X22 is the connector for the ROM selections. All signals ROM select signals of the FPGA are connected to X22. (pos. 1 of this connector is located in direction of the extension port).

X24 is an extension plug and X19 the connector for the MIDI ACIA (refer to paragraph Solder Pads SJ1 and SJ2).

X27 The extension port is functionally identical to the header of MEGA STs. The connector is reduced due to space restrictions to a 1,27mm pitch type. It is an industrial type.

X32 is the terminal for the alarm signal of the real time clock. Looking from the front at the three terminals the assignments are as follows (from left to right): interrupt - ground – alarm.

X33 is another extension plug which carries out some system signals.

X44 is intended for connecting simple monochrome LCDs which were used in ST-Books or Stacy machines. The Suska-III-C IP core supports LCDs with a VGA video resolution such that the Atari monochrome video information with 640x400 dots is displayed with black shoulders on top and bottom of the LCD.

System Modifications

Suska-III-C has three micro controllers, a nonvolatile Flash memory device and the FPGA. This means, that the system is highly configurable and enhanceable. Modifications are fairly simple to install whereas preparation or the building of the components requires some experience in hardware and/or software development. It is not recommended for inexperienced people to implement changes to the system but rather to use IP core components made publicly available for the Suska-III-C hardware. Changing the content of the flash device is normally reserved for exchanging operating system. Changes to the FPGA configuration affect the behavior of the system hardware and changes of the micro controllers supplements or exchange of the system firmware.

Loading the Operating System via the Bootloader Mechanism

The boot loader is used to copy different operating systems to the Flash memory device. This section describes how to copy an operating system image from a PC into the flash device using the X47 debugging interface of the IC39 system micro controller.

To set-up the communication between the PC and Suska-III-C connect a USB UART cable between a USB port of the PC and the debugging interface 'SYSCTRL_DEBUG' X47. This cable is available as an accessory to Suska-III-C. To activate the boot loader mechanism proceed as follows:

1. Switch on the system with push button SW7.
2. After this, press SW7 again and hold it.
3. While holding SW7 button in it's active state, press the core reset push button SW8 and release (SW8) again.
4. Release SW7.
5. Now the red boot LED should flash. The boot loader is activated when SW7 is pressed and immediately released again. If this is not done, the result is a timeout after about 3s and the boot loader is inactivated. Once activated, the red boot LED should permanently flash with a frequency of about 2Hz. In this state, the boot loader logic is waiting for communication with the PC.
Remark: is the boot loader active but there is no communication with the PC the process can be canceled by pressing SW8 (the core reset button).

6. To copy the operating system to the Flash device it is recommended to use the program 'suska-flasher'. This is a Linux program and can be started from a Linux live CD or a natively installed Linux system. The program is used via a terminal. It is necessary to change to the directory where the program 'suska-flasher' is found. Depending on the the number of operating systems to be copied to the Flash device, there are several options for 'suska-flasher'. A help screen can be displayed using the following syntax: `./suska-flasher -h` or `./suska-flasher --help`.

To have access to the USB interface, it may be required to start 'suska-flasher# in the supervisor mode. The following examples illustrate the most common variations using 'suska-flasher'. It is assumed that the operating system images are in a directory /home/myaccount/temp:

Copying the operating system (the Flash device will be erased):

```
./suska-flasher -s -v /dev/ttyUSB0 "/home/myaccount/temp/etos512k.img"
```

Copying the operating system (the Flash device will not be erased, select the address offset):

```
./suska-flasher -s -n -v /dev/ttyUSB0 "/home/myaccount/temp/tos100de.img"
```

7. If step 6 successfully invoked, the flash device will initially be erased (if this option is selected). This may take up to one minute. After this procedure copying the operating system image is begun. There is a progress bar with 'suska-flasher' to give information about the current status of the data transfer. After the data transfer has finished, switch off the system and disconnect the USB UART cable. Suska-III-C is ready for operation.

Loading the Operating System via SD Card (currently not implemented)

The boot loader mechanism allows copying several operating system images to the Flash device. This paragraph describes how to copy an operating system image from a SD card to the Flash memory. First, an enhanced functionality of the Suska-III-C IP core is required, which will be provided in a later version of 2K9A. This documentation will be updated at that time.

Loading the FPGA IP-Core

Suska-III-C comes already configured with an operable IP core located in the FPGA boot device. When the system is powered on, the FPGA device configures itself by reading the wiring configuration out of the boot device. This may take up to 0.5s. After that, the system is ready to use and represents the computer architecture of an Atari STE with enhanced video modes.

In normal use there is no need to apply changes to the FPGA configuration. However, if special functions or enhancements are to be implemented, it is necessary to change the contents of the boot device. This can be done in three different ways; by copying the IP core configuration file from a SD card to the boot device or by direct programming the boot device with the 'active serial' protocol, or by copying the wiring information directly to the configuration memory of the FPGA.

The third option can be accomplished using the JTAG interface (**J**oint **T**est **A**ction **G**roup). It has the advantage, that the FPGA reboots from the original configuration located in the boot device should the SRAM technology of the FPGA configuration memory the wiring information get lost if the system is switched off and if powered on again. This is especially useful, if changes are to be tested without risk of damage to the system's functionality.

For active serial and JTAG a special programming adapter required. Either the 'Byte Blaster' (used at the parallel port of a PC), or the 'USB Blaster' (used at any USB port). These programming adapters are accessories and available from Inventronik GmbH.

Remark: To bring in the wiring information into the boot device of the FPGA is called programming the boot device. To bring in the wiring information directly into the configuration memory of the FPGA is called to configure the FPGA. On the FPGA there is no program running (like in micro controllers) but the information to arrange the digital logic is done by the wiring of the device (configuration), the loading of the information from the boot device to the FPGA is also called configuration.

Loading the FPGA IP Core via SD Card (currently not implemented)

Later ...

Loading the FPGA IP Core via the Active Serial Interface

To do this, connect the 'USB Blaster' or the 'Byte Blaster' to the appropriate interface of a PC and to the 'ASISP' interface (X3).



Figure 20: Connecting a USB Blaster to the Active Serial Interface.

Use the Altera software Quartus or the stand-alone programming software (also available from Altera) on the PC for this purpose. To start the programmer tool look in the menu 'Tools', for the entry 'Programmer'. The use of this software is self-explanatory and supported by a detailed help system. In principle programming of the boot device is accomplished with the following steps:

- Chose the hardware for example 'USB Blaster'.
- Change the programming mode to Active-Serial.
- Choose the desired programming file x.pof.
- Choose the programming options for example Program/Configure or Verify..
- Start the programming / configuration.

Loading the FPGA IP Core via JTAG

Configuration of the FPGA via the JTAG interface is very similar to programming the boot device using the active serial interface. The difference is the setting the programming mode to JTAG and the file extension of the configuration file should be .sof. The configuration programmed via the JTAG interface is valid as long as the system is powered on even if the RESET or the SYS-RESET switches are asserted.

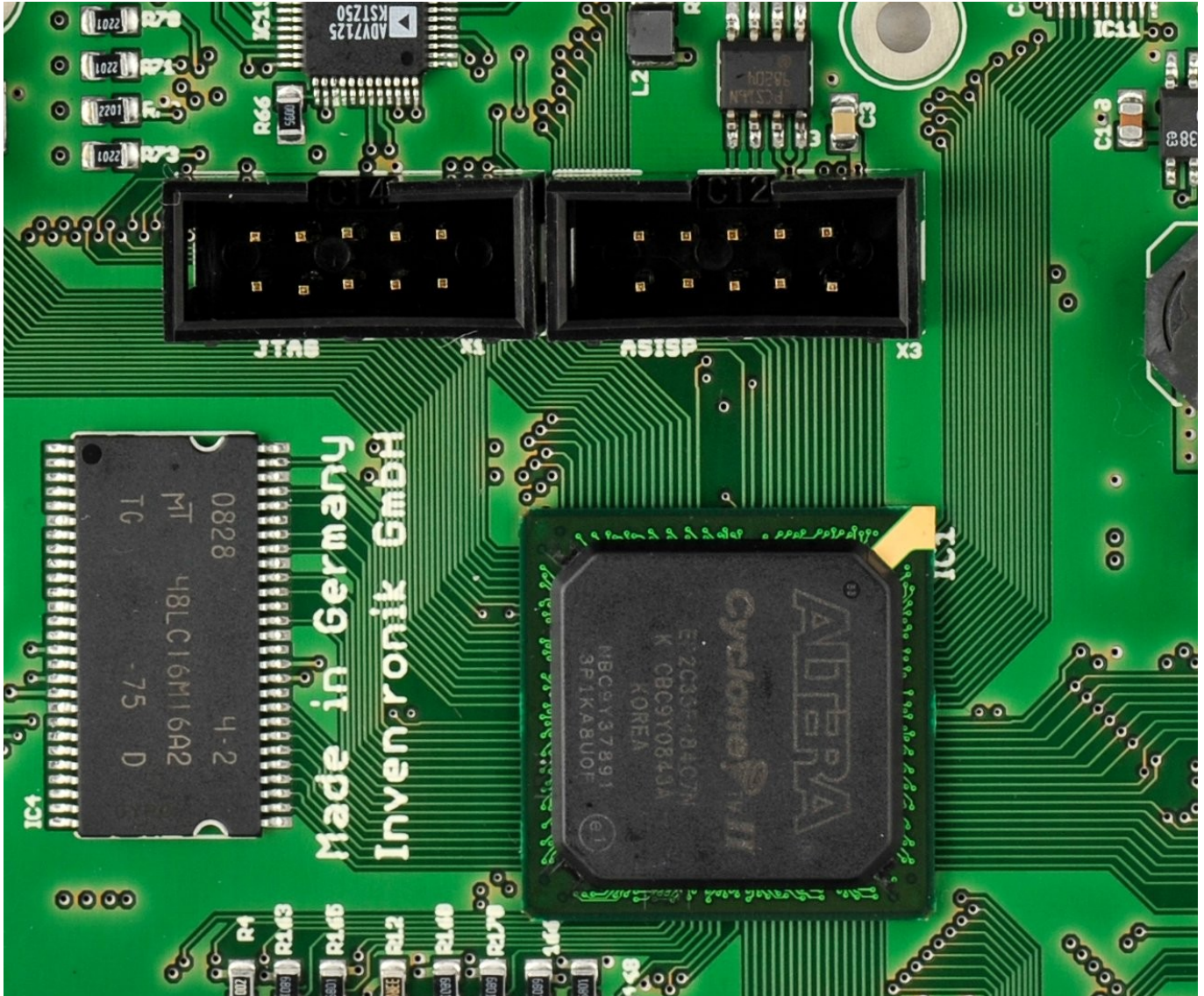


Figure 21: Configuration Interface JTAG (left) and Active Serial Programming Interface.

Programming Firmware to the Micro Controllers

The Suska-III-C hardware is equipped with three Atmel micro controllers. The programming procedure is the same for all three devices. First the programmer hardware is connected to any USB interface on the development PC and the respective programming interface of the micro controller. For the system micro controller IC39 it is the connector 'ISP_SYSCTRL' (X46), for the PS/2 micro controller IC36 it is 'ISP_PS2' (X38) and for the SD card micro controller IC37 it is 'ISP_SDC' (X42). Please take care to check the correct polarity. Terminal 1 is marked red at the programmer cable. The following figure gives an example:

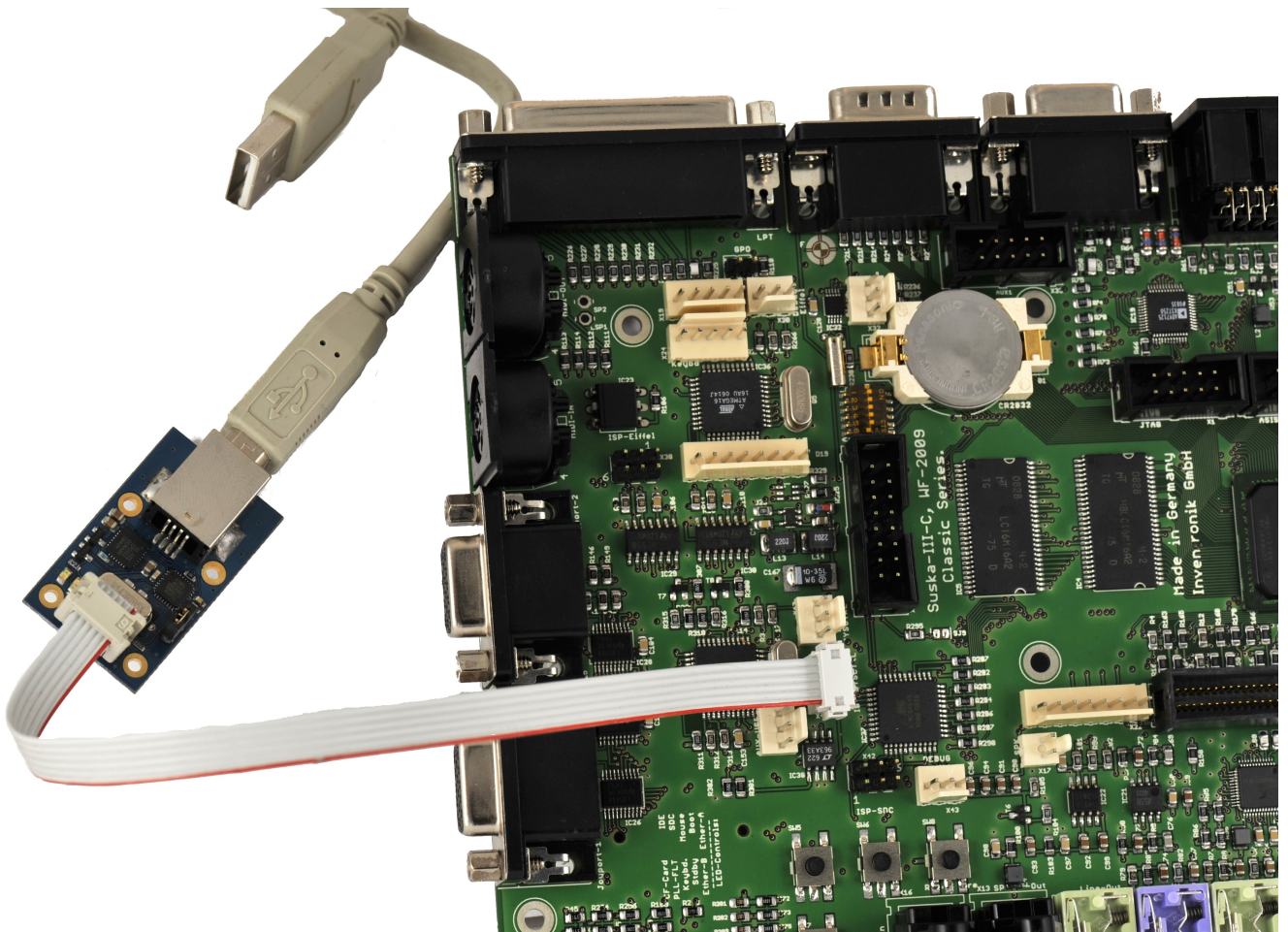


Figure 22: Connecting the AVR Programmer to Suska-III-C

Appendix1: Terminal Assignments of the Connectors

I²C X2

Pin 1	I2C_SDA
Pin 2	GND
Pin 3	I2C_SCL

Table 2: Assignment of the I2C Interface X2

ACSI X4

Pin 1	ACSI_D7
Pin 2	GND
Pin 3	ACSI_D6
Pin 4	GND
Pin 5	ACSI_D5
Pin 6	GND
Pin 7	ACSI_D4
Pin 8	GND
Pin 9	ACSI_D3
Pin 10	GND
Pin 11	ACSI_D2
Pin 12	GND
Pin 13	ACSI_D1
Pin 14	GND
Pin 15	ACSI_D0
Pin 16	GND
Pin 17	VCCIO
Pin 18	GND
Pin 19	VCC
Pin 20	ACSI_HDACKn
Pin 21	ACSI_HDREQ
Pin 22	ACSI_HDCSn
Pin 23	ACSI_RESn
Pin 24	ACSI_CA1
Pin 25	ACSI_HDINTn
Pin 26	ACSI_CR_Wn

Table 3: Assignment of the ACSI Interface X4

SCSI X5

Pin 1	SCSI_REQn
Pin 2	SCSI_MSGn
Pin 3	SCSI_IOn
Pin 4	SCSI_RSTn
Pin 5	SCSI_ACKn
Pin 6	SCSI_BUSYn
Pin 7	GND
Pin 8	SCSI_D0
Pin 9	GND
Pin 10	SCSI_D3
Pin 11	SCSI_D5
Pin 12	SCSI_D6
Pin 13	SCSI_D7
Pin 14	GND
Pin 15	SCSI_DCn
Pin 16	GND
Pin 17	SCSI_ATNn
Pin 18	GND
Pin 19	SCSI_SELn
Pin 20	SCSI_DPn
Pin 21	SCSI_D1
Pin 22	SCSI_D2
Pin 23	SCSI_D4
Pin 24	GND
Pin 25	TERM

Table 4: Assignment of the SCSI Interface X5

IDE X7: Standard Assignment

When drives in cable select mode are used, this interface is configured master.

(Connector type on the PCB: MA22-2_RM2 from Samtec)

VGA X8

Pin 1	VIDEO_R
Pin 2	VIDEO_G
Pin 3	VIDEO_B
Pin 4	n.c.
Pin 5	GND
Pin 6	GND
Pin 7	GND
Pin 8	GND
Pin 9	n.c.
Pin 10	GND
Pin 11	n.c.
Pin 12	n.c.
Pin 13	HSYNCn
Pin 14	VSYNCn
Pin 15	n.c.

Table 5: Assignment of the VGA connector X8

Atari Video X9

Pin 1	AUDIO_OUT
Pin 2	COMP_SYNC
Pin 3	CRT_PIN3
Pin 4	CRT_PIN4
Pin 5	AUDIO_IN
Pin 6	VIDEO_G
Pin 7	VIDEO_R
Pin 8	VCC via 1K2
Pin 9	HSYNCn
Pin 10	VIDEO_B
Pin 11	VIDEO_MONO
Pin 12	VSYNcn
Pin 13	GND

Table 6: Assignment of the Atari Video Connector X9

Speaker X17

Pin1 = Audio, Pin 2 = GND

GPO X18

Pin1 = GPO, Pin2 = GND

MIDI X19

Pin 1	GND
Pin 2	UART_MIDI_RTSn
Pin 3	UART_MIDI_DCDn
Pin 4	UART_MIDI_CTSn
Pin 5	VCCIO

Table 7: Assignment of the MIDI Plug X19

MIDI-In X20

Pin 1	n.c.
Pin 2	n.c.
Pin 3	n.c.
Pin 4	Optocoupler-Diode-Anode
Pin 5	Optocoupler-Diode-Cathode

Table 8: Assignment of the MIDI-In Plug X20

MIDI-Out X21

Pin 1	VCC via 220R0
Pin 2	GND
Pin 3	MIDI_TLR
Pin 4	VCC via 220R0
Pin 5	MIDI_OLR

Table 9: Assignment of the MIDI-Out Plug X21

ROM Selects X22

Pin 1	ROM0n
Pin 2	ROM1n
Pin 3	ROM2n
Pin 4	ROM3n
Pin 5	ROM4n
Pin 6	ROM5n
Pin 7	ROM6n
Pin 8	Masse

Table 10: Assignment of the ROM Selects Connector X22

Atari KBD X23

Pin 1	VCC
Pin 2	VCC
Pin 3	KEYB_TxD
Pin 4	KEYB_RxD
Pin 5	GND
Pin 6	GND

Table 11: Assignment of the Atari Keyboard Connector X23

AUX1 X24

Pin 1	GND
Pin 2	IC39_PB1
Pin 3	S/P-DIF Signal vom optischen Empfänger.
Pin 4	IC39_PC4
Pin 5	VCCIO

Table 12: Assignment of the AUX1 Interface X24

Joyport 2 X25

Pin 1	DATA3
Pin 2	DATA2
Pin 3	DATA1
Pin 4	DATA0
Pin 5	MONOFLOP3
Pin 6	BUTTON3
Pin 7	VCC
Pin 8	n.c.
Pin 9	GND
Pin 10	BUTTON3
Pin 11	DATA11
Pin 12	DATA10
Pin 13	DATA9
Pin 14	DATA8
Pin 15	MONOFLOP4

Table 13: Assignment of the Joyport2 Interface X25

Joyport 1 X26

Pin 1	DATA7
Pin 2	DATA6
Pin 3	DATA5
Pin 4	DATA4
Pin 5	MONOFLOP1
Pin 6	BUTTON1
Pin 7	VCC
Pin 8	n.c.
Pin 9	GND
Pin 10	BUTTON2
Pin 11	DATA15
Pin 12	DATA14
Pin 13	DATA13
Pin 14	DATA12
Pin 15	MONOFLOP2

Table 14: Assignment of the Joyport1 Interface X25

Extension X27; (Connector type on the PCB: TML-132 from Samtec)

Pin 1	DATA0
Pin 2	ADR23
Pin 3	DATA1
Pin 4	ADR22
Pin 5	DATA2
Pin 6	ADR21
Pin 7	DATA3
Pin 8	ADR20
Pin 9	DATA4
Pin 10	ADR19
Pin 11	DATA5
Pin 12	ADR18
Pin 13	DATA6
Pin 14	ADR17
Pin 15	DATA7
Pin 16	ADR16
Pin 17	DATA8
Pin 18	ADR15
Pin 19	DATA9
Pin 20	ADR14
Pin 21	DATA10
Pin 22	ADR13
Pin 23	DATA11
Pin 24	ADR12
Pin 25	DATA12
Pin 26	ADR11
Pin 27	DATA13
Pin 28	ADR10
Pin 29	DATA14
Pin 30	ADR9
Pin 31	DATA15
Pin 32	ADR8
Pin 33	HALTn
Pin 34	ADR7

Pin 35	BRn
Pin 36	ADR6
Pin 37	BGACKn
Pin 38	ADR5
Pin 39	DTACKn
Pin 40	ADR4
Pin 41	VPA _n
Pin 42	ADR3
Pin 43	BERR _n
Pin 44	ADR2
Pin 45	EINT7 _n
Pin 46	ADR1
Pin 47	EINT5 _n
Pin 48	RESET _n
Pin 49	EINT3 _n
Pin 50	VMA _n
Pin 51	FC2
Pin 52	E
Pin 53	FC1
Pin 54	BGO _n
Pin 55	FC0
Pin 56	CLK8
Pin 57	RW _n
Pin 58	AVEC _n
Pin 59	LDS _n
Pin 60	GND
Pin 61	UDS _n
Pin 62	GND
Pin 63	AS _n
Pin 64	GND

Table 15: Assignment of the Extension Connector X27

Rom-Port (Cartridge) X28; (Connector type on the PCB: TML-120RA from Samtec)

Pin 1	VCCIO
Pin 2	GND
Pin 3	DATA14
Pin 4	DATA15
Pin 5	DATA12
Pin 6	DATA13
Pin 7	DATA10
Pin 8	DATA11
Pin 9	DATA8
Pin 10	DATA9
Pin 11	DATA6
Pin 12	DATA7
Pin 13	DATA4
Pin 14	DATA5
Pin 15	DATA2
Pin 16	DATA3
Pin 17	DATA0
Pin 18	DATA1
Pin 19	ADR13
Pin 20	ADR15
Pin 21	ADR8
Pin 22	ADR14
Pin 23	ADR7
Pin 24	ADR9
Pin 25	ADR6
Pin 26	ADR10
Pin 27	ADR5
Pin 28	ADR12
Pin 29	ADR11
Pin 30	ADR4
Pin 31	ROM3n
Pin 32	ADR3
Pin 33	ROM4n
Pin 34	ADR2

Pin 35	UDSn
Pin 36	ADR1
Pin 37	LDSn
Pin 38	GND
Pin 39	GND
Pin 40	GND

Table 16: Assignment of the Cartridge Connector X28

Floppy Disk X29

Pin 1	FDTYPE
Pin 2	FDD_MOn
Pin 3	FDD_RDn
Pin 4	FDD_DIRCn
Pin 5	FDD_SDSEL
Pin 6	FDD_WGn
Pin 7	FDD_D1SEL
Pin 8	GND
Pin 9	FDD_TR00n
Pin 10	FDD_WPn
Pin 11	VCC
Pin 12	FDD_STEPn
Pin 13	FDD_IPn
Pin 14	FDD_WDn
Pin 15	FDD_D0SEL

Table 17: Assignment of the Floppy Connector X29

Printer Port X30

Pin 1	LPT_STRB
Pin 2	LPT_D0
Pin 3	LPT_D1
Pin 4	LPT_D2
Pin 5	LPT_D3
Pin 6	LPT_D4
Pin 7	LPT_D5
Pin 8	LPT_D6

Pin 9	LPT_D7
Pin 10	n.c.
Pin 11	LPT_BSY
Pin 12	n.c.
Pin 13	n.c.
Pin 14	n.c.
Pin 15	n.c.
Pin 16	n.c.
Pin 17	n.c.
Pin 18	GND
Pin 19	GND
Pin 20	GND
Pin 21	GND
Pin 22	GND
Pin 23	GND
Pin 24	GND
Pin 25	GND

Table 18: Assignment of the Printer Port X30

RS232 X31

Pin 1	COM_RI
Pin 2	COM_DCD
Pin 3	COM_DTR
Pin 4	GND
Pin 5	COM_RxD
Pin 6	COM_TxD
Pin 7	COM_CTS
Pin 8	COM_RTS

Table 19: Assignment of the Connector for the serial Interface X31

ALARM X32

Pin 1	RTC_INTn
Pin 2	GND
Pin 3	RTC_SQW

Table 20: Assignment of the RTC Alarm Connectors X32

AUX2 X33

Pin 1	MWK
Pin 2	MWD
Pin 3	MWE _n
Pin 4	FCLK
Pin 5	SCSI_WR _n
Pin 6	VSYNC
Pin 7	SCSI_RD _n
Pin 8	HSYNC
Pin 9	XFF827E_D4
Pin 10	GND

Table 21: Assignment of the AUX2 Interface X33

Ethernet X34

Pin 1	TD+
Pin 2	TD-
Pin 3	RD+
Pin 4	VCCIO
Pin 5	n.c.
Pin 6	RD-
Pin 7	n.c.
Pin 8	GND

Table 22: Assignment of the Ethernet Plug X34

AUX3 X36

Pin 1	GND
Pin 2	IC36 PA0
Pin 3	IC36 PA1
Pin 4	IC36 PA2
Pin 5	IC36 PA3
Pin 6	IC36 PA4
Pin 7	IC36 PA5
Pin 8	VCC

Table 23: Assignment of the AUX3 Interface X36

PS2-MOUSE X37

Pin 1	PS2_B_D
Pin 2	n.c.
Pin 3	GND
Pin 4	VCC
Pin 5	PS2_B_CLK
Pin 6	n.c.

Table 24: Assignment of the PS/2 Mouse Connector X37

PS2_Debug X39

Pin 1	TxD
Pin 2	RxD
Pin 3	GND

Table 25: Assignment of the PS/2 Micro Controller Debugging Interface X39

PS2-KBD X40

Pin 1	PS2_A_D
Pin 2	n.c.
Pin 3	GND
Pin 4	VCC
Pin 5	PS2_A_CLK
Pin 6	n.c.

Table 26: Assignment of the PS/2 Keyboard Plug X40

SDC_Debug X43

Pin 1	TxD
Pin 2	RxD
Pin 3	GND

Table 27: Assignment of the SDC Micro Controller Debugging Connector X43

LCD X44

Pin 1	GND
Pin 2	VDCLK
Pin 3	LLCLK
Pin 4	LFS
Pin 5	GND
Pin 6	GND
Pin 7	LDAT0
Pin 8	LDAT1
Pin 9	LDAT2
Pin 10	LDAT
Pin 11	UDAT0
Pin 12	UDAT1
Pin 13	UDAT2
Pin 14	UDAT
Pin 15	LCD_VBIAS
Pin 16	VCC

Table 28: Assignment of the LCD Interface X44

AUX-USB X45

Pin 1	IC39 PA2
Pin 2	IC39 PA3
Pin 3	GND

Table 29: Assignment of the AUX-USB Interface X45

SYSCTRL_Debug X47

Pin 1	TxD
Pin 2	RxD
Pin 3	GND

Table 30: Assignment of the SYS Micro Controller Debugging Interface X47

Power X48

Center Pin = +7V bis +12V, Other Pin = GND.

Appendix 2: Keyboard Scan Codes / Translation Table

The scan codes marked in green indicate the following differences to Atari keyboards:

Pos 1 = CtrHome, Pause = Undo, Druck = Help,

Not used = '(' Number Pad, Not used = ')' Number Pad.

Scan Code	Key D	Scan Code	Key D	Scan Code	Key D	Scan Code	Key D
1	ESC	35	H	69	Not used	103	7 Number Pad
2	1	36	J	70	Not used	104	8 Number Pad
3	2	37	K	71	Pos1, CtrHome	105	9 Number Pad
4	3	38	L	72	↑	106	4 Number Pad
5	4	39	Ö	73	Not used	107	5 Number Pad
6	5	40	Ä	74	- Number Pad	108	6 Number Pad
7	6	41	#	75	←	109	1 Number Pad
8	7	42	Shiftt left	76	Not used	110	2 Number Pad
9	8	43	~	77	→	111	3 Number Pad
10	9	44	Y	78	+ Number Pad	112	0 Number Pad
11	0	45	X	79	Not used	113	, Number Pad
12	ß	46	C	80	↓	114	Enter NumPad
13	'	47	V	81	Not used	115	Not used
14	Backspace	48	B	82	Insert	116	Not used
15	TAB	49	N	83	Delete	117	Not used
16	Q	50	M	84	Shift-F1	118	Not used
17	W	51	,	85	Shift-F2	119	Not used
18	E	52	.	86	Shift-F3	120	ALT 1
19	R	53	-	87	Shift-F4	121	ALT 2
20	T	54	Shift right	88	Shift-F5	122	ALT 3
21	Z	55	Not used	89	Shift-F6	123	ALT 4
22	U	56	Alternate	90	Shift-F7	124	ALT 5
23	I	57	Space	91	Shift-F8	125	ALT 6
24	O	58	Caps Lock	92	Shift-F9	126	ALT 7
25	P	59	F1	93	Shift-F10	127	ALT 8
26	Ü	60	F2	94	Not used	128	ALT 9
27	+	61	F3	95	Not used	129	ALT 0
28	Return	62	F4	96	<	130	ALT ß
29	Control	63	F5	97	Pause, Undo	131	ALT '
30	A	64	F6	98	Druck, Help	132	Not used

31	S	65	F7	99	n.b., (Number Pad		
32	D	66	F8	100	n.b.,)Number Pad		
33	F	67	F9	101	/ Number Pad		
34	G	68	F10	102	* Number Pad		

Appendix 3: Mega STE Configuration Switch

README to the CPX-Module "DIPS":

With this module the settings of the DIP switches of the Mega STE respective TT can be read or changed. The software overwrites the hardware settings because the settings are read once after a reset or the boot process and stored in the cookie `_SWI`. The settings can later be changed in this cookie without opening the computer. The eight switches are stored in the lower part of the `_SWI` longword. If a switch is in position 'on', the respective cookie bit is then '0' otherwise '1'. Up to now, there is information for the function of only two bits available:

Switch 8:

Off = System has DMA sound (is indicated `_SND` cookie, bit 1)

Switch 7:

Determines whether the system is equipped with (at least) one HD floppy disk drive. Since TOS 2.05/3.05 the operation of HD type floppy disk drives is possible.

More information on this topic can be found here: ST-Computer 9/91, pages 100 ff.

Appendix 4: Schematics

To have access to the most recent versions of the schematics for the Suska-III-C hardware refer to the document „Schematics_Suska-III-C_Series-1.pdf“, which is available in the download area of the experiment-s.de or the inventronik.de web site.

Appendix 5: Board Layouts

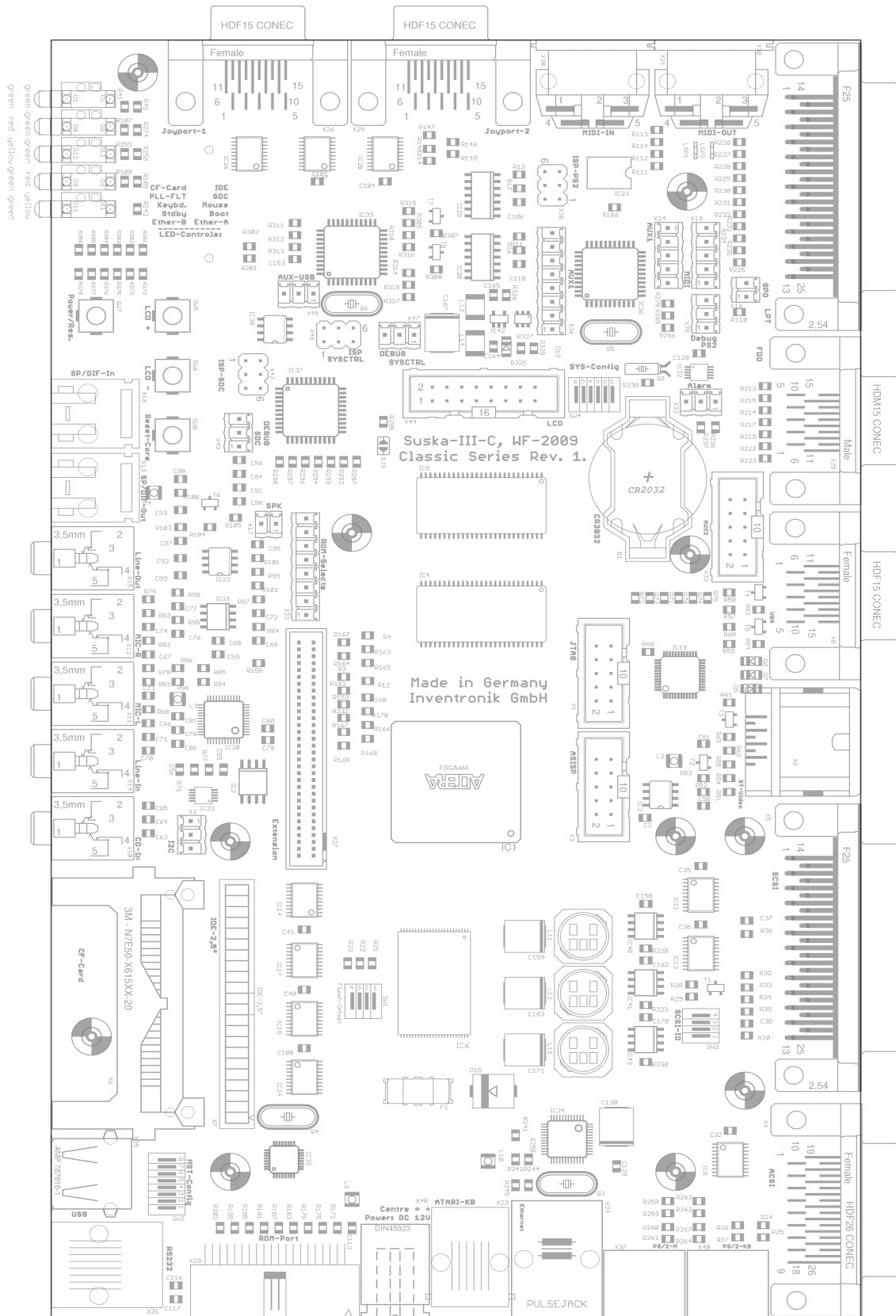


Figure 23: Suska-III-C Top View PCB Layout

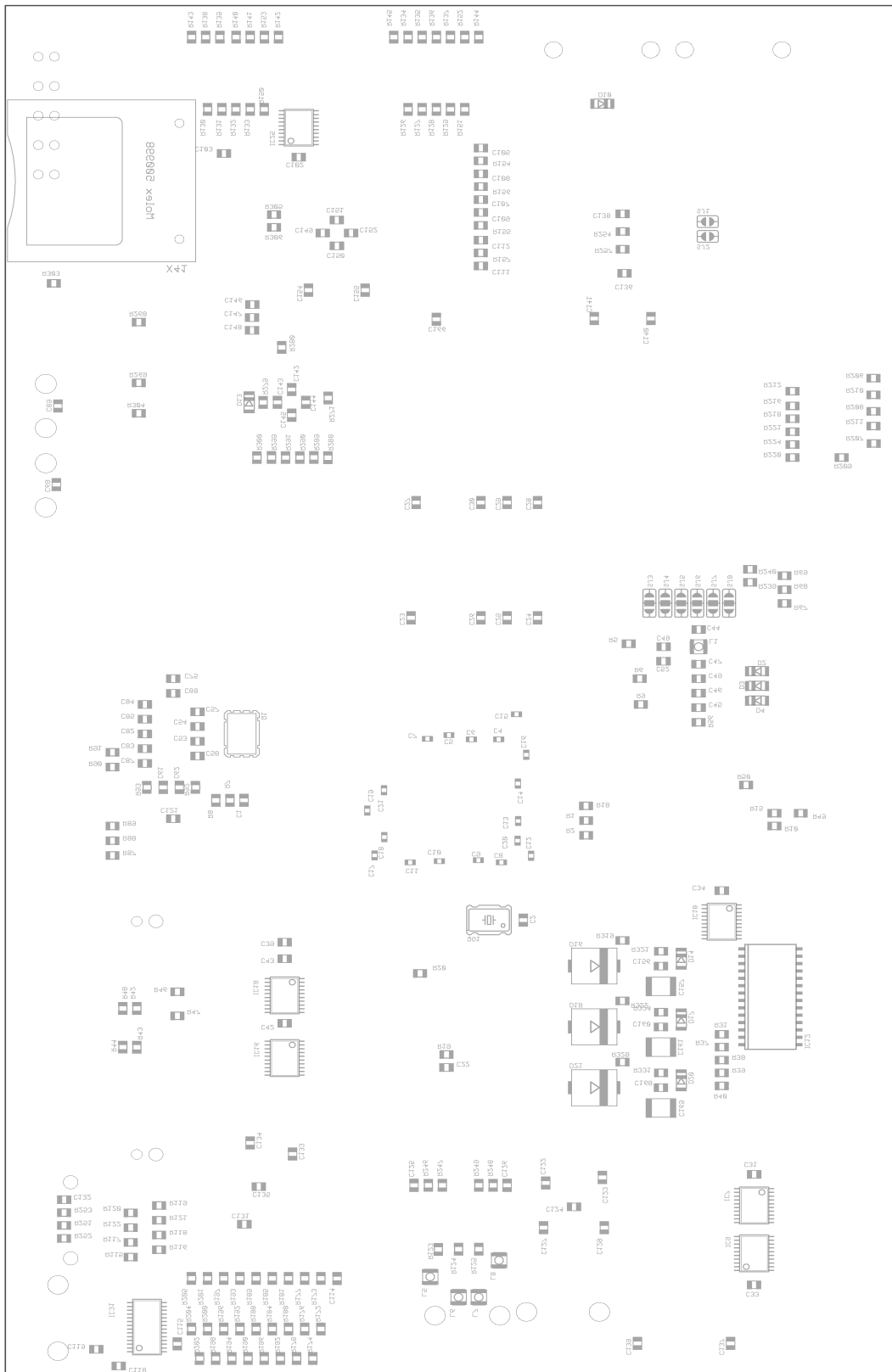


Figure 24: Suska-III-C Bottom View PCB Layout

Appendix 6: Literature

1. Siemers C.; Logikbausteine; Vogel Buchverlag; Würzburg; 2002.
2. Tischler M., Oertel K.; FPGAs und CPLDs; Hüthig GmbH; Heidelberg; 1998.
3. Reichardt J., Schwarz B.; VHDL-Synthese; Oldenbourg Wissenschaftsverlag; München; 2001.
4. Molitor P., Ritter J.; VHDL Eine Einführung; Pearson Studium; München; 2004.
5. Seifart M., Beikirch H.; Digitale Schaltungen; Verlag Technik; Berlin; 1998.
6. Lehman G., Wunder B., Selz M.; Schaltungsdesign mit VHDL; frei im Internet verfügbar.
7. Ashenden P. J.; The Designers Guide To VHDL; Morgan Kaufmann Publishers; New York; 2002.
8. Ten Hagen K.; Abstrakte Modellierung digitaler Schaltungen; Springer Verlag; Berlin; 1995.

Appendix 7: Web Links

1. Inventronik Home: www.inventronik.de
2. experiment-S Home: www.experiment-s.de
3. IP-Cores: www.opencores.org
4. Funsite: www.fpgaarcade.com
5. Altera FPGAs: www.altera.com